MALLA REDDY ENGINEERING COLLEGE

(Autonomous)

LECTURE NOTES

ON

LINEAR & DIGITAL INTEGRATED CIRCUIT APPLICATIONS (80410)

B.Tech-ECE-IV semester

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ELECTRONICS AND COMMUNICATION ENGINEERING

MALLA REDDY ENGINEERING COLLEGE (Autonomous)

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2017-18 (MR-17)	MALLA REDDY ENGINEERING COLLEGE (Autonomous)	B.Tech. V Semester		
Code: 70414	**LINEAR & DIGITAL INTEGRATED CIRCUIT APPLICATIONS**	**L**	**T**	**P**
Credits: 3		**3**	**-**	**-**

Prerequisites: Switching Theory & Logic Design, Pulse & Digital Circuits.

Course Objective: This course introduces the basic op-amp IC741 and study various linear and non-linear applications of op-amps. This also introduces the types of filters, timers and PLLs and their implementation and to design regulators, D-A & A-D converters and combinational & sequential logic circuits.

UNIT – I **[8 Periods]**

INTEGRATED CIRCUITS AND OPERATIONAL AMPLIFIER: Introduction, Classification of IC's, IC chip size and circuit complexity, basic information of Op-Amp, IC741Op-Amp and its features, the ideal Operational amplifier, Op-Amp internal circuit, Op-Amp characteristics - DC and AC.

UNIT – II **[10 Periods]**

LINEAR APPLICATIONS OF OP-AMP: Inverting and non-inverting amplifiers, adder, subtractor, Instrumentation amplifier, AC amplifier, V to I and I to V converters, Integrator and differentiator.

NON-LINEAR APPLICATIONS OF OP-AMP: Sample and Hold circuit, Log and Antilog amplifier, multiplier and divider, Comparators, Schmitt trigger, Multivibrators, Triangular and Square waveform generators, Oscillators.

UNIT - III **[10 Periods]**

ACTIVE FILTERS: Introduction, Butterworth filters – 1st order, 2nd order low pass and high pass filters, band pass, band reject and allpass filters.

TIMER AND PHASE LOCKED LOOPS: Introduction to IC 555 timer, description of functional diagram, monostable and astable operations and applications, schmitt trigger, PLL - introduction, basic principle, phase detector/comparator, voltage controlled oscillator (IC 566), low pass filter, monolithic PLL and applications of PLL.

UNIT - IV **[10 Periods]**

VOLTAGE REGULATOR: Introduction, Series Op-Amp regulator, IC Voltage Regulators, IC 723 general purpose regulators, Switching Regulator.

D to A AND A to D CONVERTERS: Introduction, basic DAC techniques - weighted resistor DAC, R-2R ladder DAC, inverted R-2R DAC, A to D converters - parallel comparator type ADC, counter type ADC, successive approximation ADC and dual slope ADC, DAC and ADC Specifications.

UNIT – V **[10 Periods]**

CMOS LOGIC: CMOS logic levels, MOS transistors, Basic CMOS Inverter, NAND and NOR gates, CMOS AND-OR-INVERT and OR-AND-INVERT gates, implementation of function using CMOS logic.

COMBINATIONAL CIRCUITS USING TTL *74XX* ICS: Study of logic gates using *74XX* ICs, Four-bit parallel adder(IC 7483), Comparator(IC 7485), Decoder(IC 74138, IC 74154), BCD-to-7-segment decoder(IC 7447), Encoder(IC 74147), Multiplexer(IC 74151), Demultiplexer (IC 74154).

SEQUNTIAL CIRCUITS USING TTL *74XX* ICS: Flip Flops (IC 7474, IC 7473), Shift Registers, Universal Shift Register(IC 74194), 4- bit asynchronous binary counter(IC 7493).

TEXT BOOKS:

1. D. Roy Choudhury, Shail B. Jain (2012), Linear Integrated Circuit, 4th edition, New Age International Pvt. Ltd., New Delhi, India.
2. Ramakant A. Gayakwad, (2012), OP-AMP and Linear Integrated Circuits, 4th edition, Prentice Hall / Pearson Education, New Delhi.
3. Floyd, Jain (2009), Digital Fundamentals, 8th edition, Pearson Education, New Delhi.

REFERENCE BOOKS:

1. Sergio Franco (1997), Design with operational amplifiers and analog integrated circuits, McGraw Hill, New Delhi.
2. Gray, Meyer (1995), Analysis and Design of Analog Integrated Circuits, Wiley International, New Delhi.
3. John F. Wakerly (2007), Digital Design Principles and practices, Prentice Hall / Pearson Education, New Delhi.

Text Books:

1. S. Salivahanan, N Suresh Kumar, "Electronic Circuit Analysis", Tata McGraw Hill Education Private Limited, New Delhi, 2ndEdition, 2012.
2. Jacob Milliman, Christos C. Halkias, Chetan D. Parikh "Integrated Electronics - Analog and Digital Circuits and Systems", Tata McGraw Hill Education Private Limited, New Delhi, 2ndEdition, 2011

Reference Books:

1. G. K. Mithal, "Electronic Devices and Circuits", Khanna Publishers, New Delhi, 2nd Edition, 1998.
2. David A. Bell "Solid state pulse circuits", Prentice Hall of India, New Delhi, India. 4th Edition, 2002.

E-RESOURCES:

1. http://fmcet.in/ECE/EC6404_uw.pdf
2. https://www.iare.ac.in/sites/default/files/lecture_notes/LDIC%20Lecture%20Notes.pdf.
3. http://smec.ac.in/sites/default/files/lecture_notes/Course%20File%20of%20LDIC(Linear%20and%20Digital%20IC%20Applications).pdf
4. http://crectirupati.com/sites/default/files/lecture_notes/LDICA%20Lecture%20notes%20by%20A.Mounika.pdf
5. http://www.springer.com/engineering/electronics/journal/10470.
6. https://www.journals.elsevier.com/microelectronics-journal
7. http://nptel.ac.in/courses/117107094/
8. https://www.youtube.com/watch?v=NVj_Eu3sJL4
9. http://freevideolectures.com/Course/2915/Linear-Integrated-Circuits

MODULE I: INTEGRATED CIRCUITS AND OPERATIONAL AMPLIFIER

A simple electronic circuit can be designed easily because it requires few discrete electronic components and connections. However, designing a complex electronic circuit is difficult, as it requires more number of discrete electronic components and their connections. It is also time taking to build such complex circuits and their reliability is also less. These difficulties can be overcome with Integrated Circuits.

Integrated Circuit (IC)

If multiple electronic components are interconnected on a single chip of semiconductor material, then that chip is called as an **Integrated Circuit (IC)**. It consists of both active and passive components.

This chapter discusses the advantages and types of ICs.

Advantages of Integrated Circuits

Integrated circuits offer many advantages. They are discussed below −

- **Compact size** − For a given functionality, you can obtain a circuit of smaller size using ICs, compared to that built using a discrete circuit.
- **Lesser weight** − A circuit built with ICs weighs lesser when compared to the weight of a discrete circuit that is used for implementing the same function of IC. using ICs, compared to that built using a discrete circuit.
- **Low power consumption** − ICs consume lower power than a traditional circuit,because of their smaller size and construction.
- **Reduced cost** − ICs are available at much reduced cost than discrete circuits because of their fabrication technologies and usage of lesser material than discrete circuits.
- **Increased reliability** − Since they employ lesser connections, ICs offer increased reliability compared to digital circuits.
- **Improved operating speeds** − ICs operate at improved speeds because of their switching speeds and lesser power consumption.

Types of Integrated Circuits

Integrated circuits are of two types − **Analog Integrated Circuits and Digital Integrated Circuits**.

Analog Integrated Circuits

Integrated circuits that operate over an entire range of continuous values of the signal amplitude are called as **Analog Integrated Circuits.** These are further classified into the two types as discussed here −

- **Linear Integrated Circuits** − An analog IC is said to be Linear, if there exists a linear relation between its voltage and current. IC 741, an 8-pin Dual In-line Package (DIP)op-amp, is an example of Linear IC.

- **Radio Frequency Integrated Circuits** − An analog IC is said to be Non-Linear, if there exists a non-linear relation between its voltage and current. A Non-Linear IC is also called as Radio Frequency IC.

Digital Integrated Circuits

If the integrated circuits operate only at a few pre-defined levels instead of operating for an entire range of continuous values of the signal amplitude, then those are called as **Digital Integrated Circuits**.

In the coming chapters, we will discuss about various Linear Integrated Circuits and their applications.

Classification of ICs (Integrated Circuits)

Below is the classification of **different types of ICs** basis on their chip size.

- **SSI**: Small scale integration. 3 – 30 gates per chip.
- **MSI**: Medium scale integration. 30 – 300 gates per chip.
- **LSI**: Large scale integration. 300 – 3,000 gates per chip.
- **VLSI**: Very large scale integration. More than 3,000 gates per chip.

Types of ICs (Integrated Circuits)

Based on the method or techniques used in manufacturing them, *types of ICs* can be divided into three classes:

1. Thin and thick film ICs
2. Monolithic ICs
3. Hybrid or multichip ICs

Below is the simple explanation of different types of ICs as mentioned above.

Thin and Thick ICs:

In thin or thick film ICs, passive components such as resistors, capacitors are integrated but the diodes and transistors are connected as separate components to form a single and a complete circuit. Thin and thick ICs that are produced commercially are merely the combination of integrated and discrete (separate) components.

Thick and thin ICs have similar characteristics, similar appearance except the method of film deposition. Method of deposition of films distinguished Thin ICs from Thick ICs.

Thin film ICs are made by depositing films of a conducting material on a glass surface or on a ceramic base. By varying the thickness of the films deposited on the materials having different resistivity, Passive electronic components like resistors and capacitors can be manufactured.

In Thick film ICs, silk printing technique is used to create the desired pattern of the circuit on a ceramic substrate. Thick-film ICs are sometimes referred to as printed thin-film.

The screens are actually made of fine stainless steel wire mesh and the links (connections) are pastes having conductive, resistive or dielectric properties. The circuits are fired in a furnace at a high temperature so as to fuse the films to the substrate after printing.

Monolithic ICs

In monolithic ICs, the discrete components, the active and the passive and also the interconnections between then are formed on a silicon chip. The word monolithic is actually derived from two Greek words “mono” meaning one or single and Lithos meaning stone. Thus monolithic circuit is a circuit that is built into a single crystal.

Monolithic IC in Plastic Package (DIP)

Monolithic ICs are the most common types ICs in use today. Its cost of production is cheap and is reliable. Commercially manufactured ICs are used as amplifiers, voltage regulators, in AM receivers, and in computer circuits. However, despite all these advantages and vast fields of application of monolithic ICs, it has limitations. The insulation between the components of monolithic ICs is poor. It also have low power rating, fabrication of insulators is not that possible and so many other factors.

Advantages and Applications of ICs

ICs have advantages over those that are made by interconnecting discrete components some of which are its small size. It is a thousand times smaller than the discrete circuits. It is an all in one (components and the interconnections are on a single silicon chip). It has little weight.

Its cost of production is also low. It is reliable because there is no soldered joints. ICs consumes little energy and can easily be replaced when the need arises. It can be operated at a very high temperature. different types of ICs are widely applied in our electrical devices such as high power amplifiers, voltage regulators, TV receivers and computers etc.

Limitation for different types of ICs

Despite the advantages that ICs provide us with, it have limitations some of which are:

- Limited power rating
- It operates at low voltage
- High grade of PNP is not possible
- It produces noise during operation
- Its components such as resistors and capacitors are voltage dependent
- It is delicate i.e it cannot withstand rough handling etc.

Basics Of Operational Amplifier

Operational Amplifier, also called as an Op-Amp, is an integrated circuit, which can be used to perform various linear, non-linear, and mathematical operations. An op-amp is a **direct coupled high gain amplifier**. You can operate op-amp both with AC and DC signals. This chapter discusses the characteristics and types of op-amps.

Construction of Operational Amplifier

An op-amp consists of differential amplifier(s), a level translator and an output stage. A differential amplifier is present at the input stage of an op-amp and hence an op-amp consists of **two input terminals**. One of those terminals is called as the **inverting terminal** and the other one is called as the **non-inverting terminal**. The terminals are named based on the phase relationship between their respective inputs and outputs.

Characteristics of Operational Amplifier

The important characteristics or parameters of an operational amplifier are as follows −

- Open loop voltage gain
- Output offset voltage
- Common Mode Rejection Ratio
- Slew Rate

This section discusses these characteristics in detail as given below −

Open loop voltage gain

The open loop voltage gain of an op-amp is its differential gain without any feedback path.

Mathematically, the open loop voltage gain of an op-amp is represented as −

$$Av=v_0/(v_1−v_2)$$

Output offset voltage

The voltage present at the output of an op-amp when its differential input voltage is zero is called as **output offset voltage.**

Common Mode Rejection Ratio:

Common Mode Rejection Ratio (**CMRR**) of an op-amp is defined as the ratio of the closed loop differential gain, AdAd and the common mode gain, AcAc.

Mathematically, CMRR can be represented as −

$$CMRR=AdAcCMRR=AdAc$$

Note that the common mode gain, AcAc of an op-amp is the ratio of the common mode output voltage and the common mode input voltage.

Slew Rate:

Slew rate of an op-amp is defined as the maximum rate of change of the output voltage due to a step input voltage.

Mathematically, slew rate (SR) can be represented as −

$$SR=\text{Maximum of } (dV_0/dt)$$

Types of Operational Amplifiers:

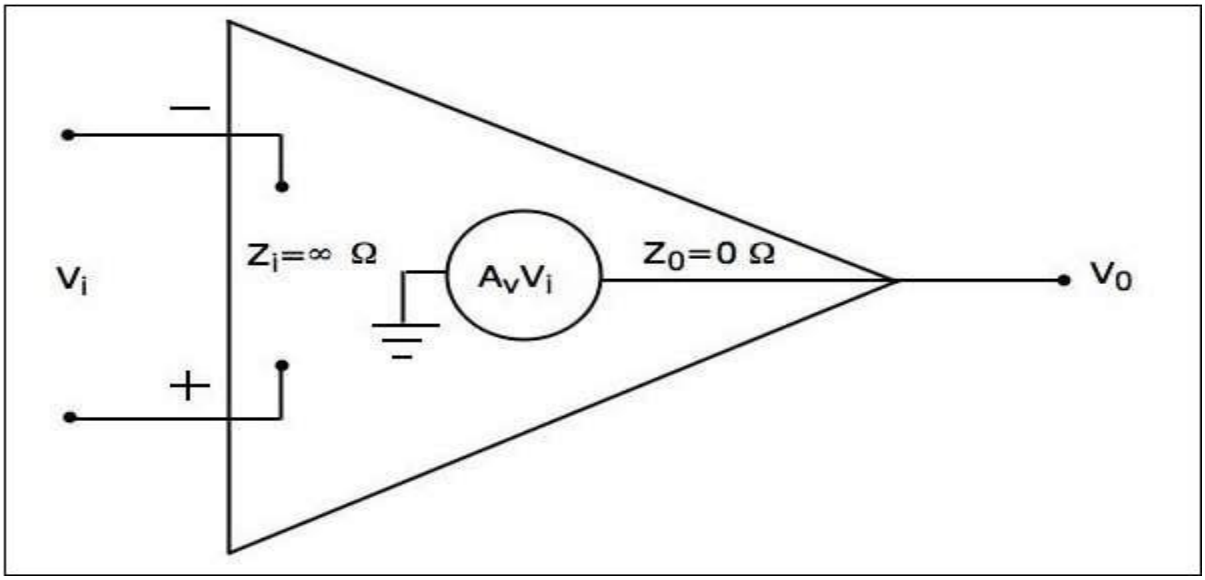
An op-amp is represented with a triangle symbol having two inputs and one output.

Op-amps are of two types: **Ideal Op-Amp** and **Practical Op-Amp**.

They are discussed in detail as given below −

Ideal Op-Amp

An ideal op-amp exists only in theory, and does not exist practically. The **equivalent circuit** of an ideal op-amp is shown in the figure given below −

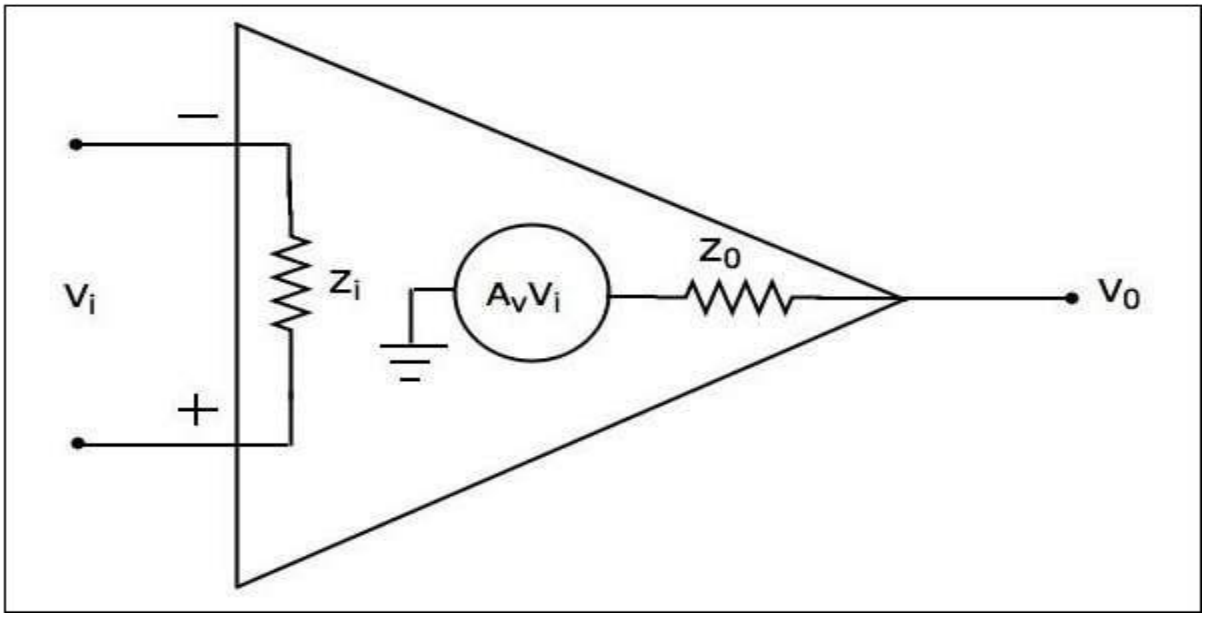


An **ideal op-amp** exhibits the following characteristics −

- Input impedance Zi=∞Ω
- Output impedance Z0=0Ω
- Open loop voltage gaine Av=∞
- If (the differential) input voltage Vi=0V, then the output voltage will be V0=0V.
- Bandwidth is **infinity**. It means, an ideal op-amp will amplify the signals of any frequency without any attenuation.
- Common Mode Rejection Ratio **(CMRR)** is **infinity**.
- Slew Rate **(SR)** is **infinity**. It means, the ideal op-amp will produce a change in the output instantly in response to an input step voltage.

Practical Op-Amp

Practically, op-amps are not ideal and deviate from their ideal characteristics because of some imperfections during manufacturing. The **equivalent circuit** of a practical op-amp is shown in the following figure −



A **practical op-amp** exhibits the following characteristics −

- Input impedance, Z_i in the order of **Mega ohms**.
- Output impedance, Z_0 in the order of **fewohms.**.
- Open loop voltage gain, Av will be **high**.

When you choose a practical op-amp, you should check whether it satisfies the following conditions −

- Input impedance, Zi should be as high as possible.
- Output impedance, Z0 should be as low as possible.
- Open loop voltage gain, Av should be as high as possible.
- Output offset voltage should be as low as possible.
- The operating Bandwidth should be as high as possible.
- CMRR should be as high as possible.
- Slew rate should be as high as possible.

Note − IC 741 op-amp is the most popular and practical op-amp.

AC and DC performance characteristics of op-amp in detail.

Dc characteristics: An ideal op- amp draws no current from the source and its response is also independent of temperature. However, a real op-amp does not work this way. Current is taken from the source into the op-amp inputs. Also the inputs respond differently to current and voltage due to mismatch in transistors. A real op-amp also shifts its operation with temperature. These non- ideal dc characteristics that add error components to the dc output voltage are:

1. Input bias current

2. Input offset current

3. Input offset voltage

4. Thermal drift

1. Input bias current: It is defined as the average value of the base currents entering into the input terminals of an op-amp during the input bias current. The op-amp input is a differential amplifier, which may be made of BJT or FET. In either case, the input transistors must be biased into their linear region by supplying 7 currents into the bases by the external circuit.

In an ideal op-amp we assume that no current is drawn from the input terminals. However, practically, input terminals do conduct a small value of dc current to bias the input transistors. The base currents entering into the inverting and non-inverting terminals are shown as IB^ (-) and IB^ (+) respectively. Even though both the transistors are identical, IB^ (-) and IB^ (+) are not exactly equal due to internal imbalances between the two inputs.

IB= IB^ (+) + IB^ (-)/ 2 ,Where IB^ (+) – bias current at non- inverting terminal IB (-) - bias current at inverting terminal Input bias current compensation: IB for BJT is 500mA• IB for FET is 50pA• By introducing compensation resistor at the non-inverting input terminal we can able to reduce the input bias current. Rcomp=R1/ Rf= (R1* Rf) / (R1+Rf)

2. Input offset current: Bias current compensation will work efficiently if both the bias currents IB^ (+) and IB^ (-) are equal. The input transistors cannot be made identical. Hence there will be difference in bias currents. This difference is called as input offset current Ios and can be written as | Ios | = IB^ (+) – IB^ (-) The absolute value sign indicates that there is no way to predict which of the bias currents will be larger. Input offset current for BJT is 200nA. Input offset current for FET is 10pA. The effect of Ios can be minimized by having the feedback resistor value to be small.

3. Input offset voltage: In spite of the use of the above compensation techniques, it is found that the output voltage may still not be zero with zero input voltage. This is due to unavoidable imbalances inside the op-amp and one may have to apply a small voltage at the input terminals to make output voltage zero. This voltage is called input offset voltage Vios. This is the voltage required to be applied at the input for making output voltage to zero volts. The voltage V2 at negative terminal is V2 =R 1.V0/R1+Rf Or V0 = (R1 +Rf)V2/R1 = (1+ Rf/R1)V2 Since VOS = |Vi –V2| and Vi = 0 VOS = |0 –V2| = V2

4. Thermal drift: Bias current, offset current and offset voltage change with temperature. A circuit carefully mulled at 25 degree Celsius may not remain so when the temperature rises to 35 degree Celsius. This is called drift. Often, offset current drift is expressed in nA/0C and offset voltage drift in mV/0C.

These indicate the change in offset for each degree Celsius change in temperature. 8 There are very few circuit techniques that can be used to minimize the effect of drift. Careful printed circuit board layout must be equal be used to keep op-amps away from source of heat. Forced air cooling may be used to stabilize the ambient temperature.

Ac characteristics:

For small signal sinusoidal applications the a.c. characteristics are

1. Frequency response

2. Slew rate

1. Frequency response: An ideal op-amp has infinite band width that is open loop gain is 90dB with d.c.signal and this gain should remain the same through audio and radio frequency. But practically op-amp gain decreases at high frequency. This is due to a capacitive component in the equivalent circuit of op-amp. Due to R0C, the gain decreases by 20 dB per decay and the frequency is said to be brake or corner frequency and is given by f1= 1/ (2*3.14*R0*C) |A|= A0*L/ (1+ (f/f1) ^2)

2. Slew rate: The slew rate is defined as the maximum rate of change of output voltage caused by a step input voltage and is usually specified in V/µs. for e.g. A 1V/µs slew rate means that the output rises or falls by 1V in one 1µs. The rate of change of output voltage due to the step input voltage and is usually specified as V/micro sec. For example: 1V/micro sec. slew rate denotes the output rises or falls by 1 volts in 1 micro seconds. The rate at which the voltage across the capacitor dVc/dt is given by dVc/dt = I/C Slew rate SR dVc/dt|max= Imax/ C For IC741 Imax= 15 micro amps, C= 30 Pico farad Slew rate = 0.5V/ micro sec.

MODULE II: LINEAR & NON-LINEAR APPLICATIONS OF OP-AMP

Op-Amp-Applications

A circuit is said to be **linear**, if there exists a linear relationship between its input and the output. Similarly, a circuit is said to be **non-linear**, if there exists a non-linear relationship between its input and output.

Op-amps can be used in both linear and non-linear applications. The following are the basic applications of op-amp −

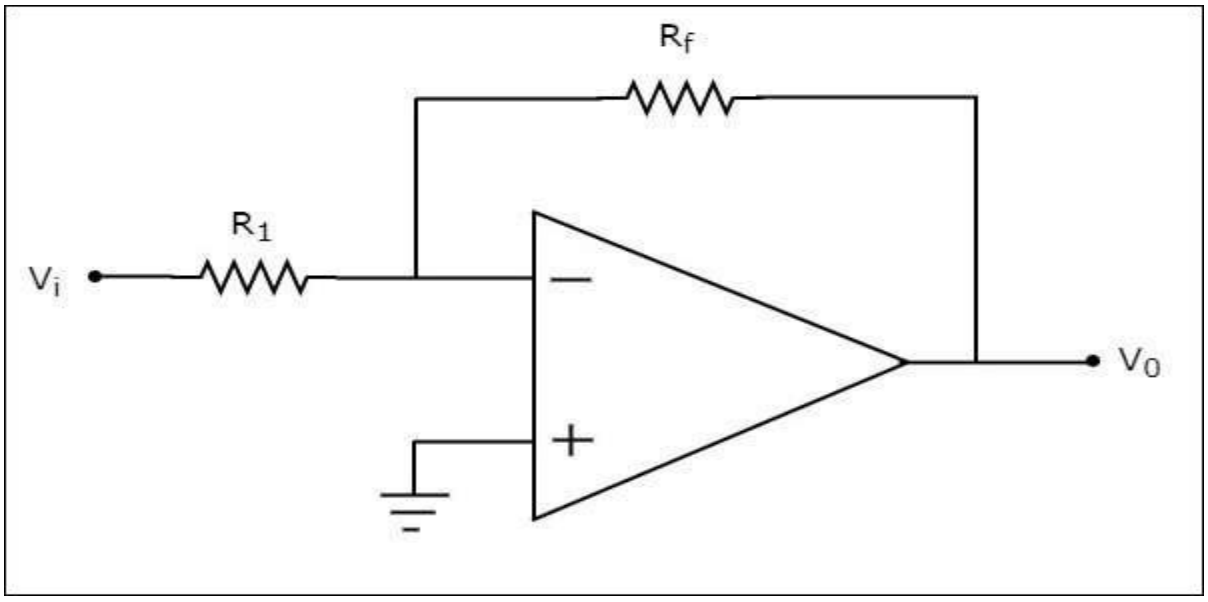
- Inverting Amplifier
- Non-inverting Amplifier
- Voltage follower

This chapter discusses these basic applications in detail.

Inverting Amplifier

An inverting amplifier takes the input through its inverting terminal through a resistor R1R1, and produces its amplified version as the output. This amplifier not only amplifies the input but also inverts it (changes its sign).

The **circuit diagram** of an inverting amplifier is shown in the following figure −



Note that for an op-amp, the voltage at the inverting input terminal is equal to the voltage at its non-inverting input terminal. Physically, there is no short between those two terminals but **virtually**, they are in **short** with each other.

In the circuit shown above, the non-inverting input terminal is connected to ground. That means zero volts is applied at the non-inverting input terminal of the op-amp.

According to the **virtual short concept**, the voltage at the inverting input terminal of an op-amp will be zero volts.

The **nodal equation** at this terminal's node is as shown below −

$$0-ViR1+0-V0Rf=00-ViR1+0-V0Rf=0$$

$$=>-ViR1=V0Rf=>-ViR1=V0Rf$$

$$=>V0=(-RfR1)Vt=>V0=(-RfR1)Vt$$

$$=>V0Vi=-RfR1=>V0Vi=-RfR1$$

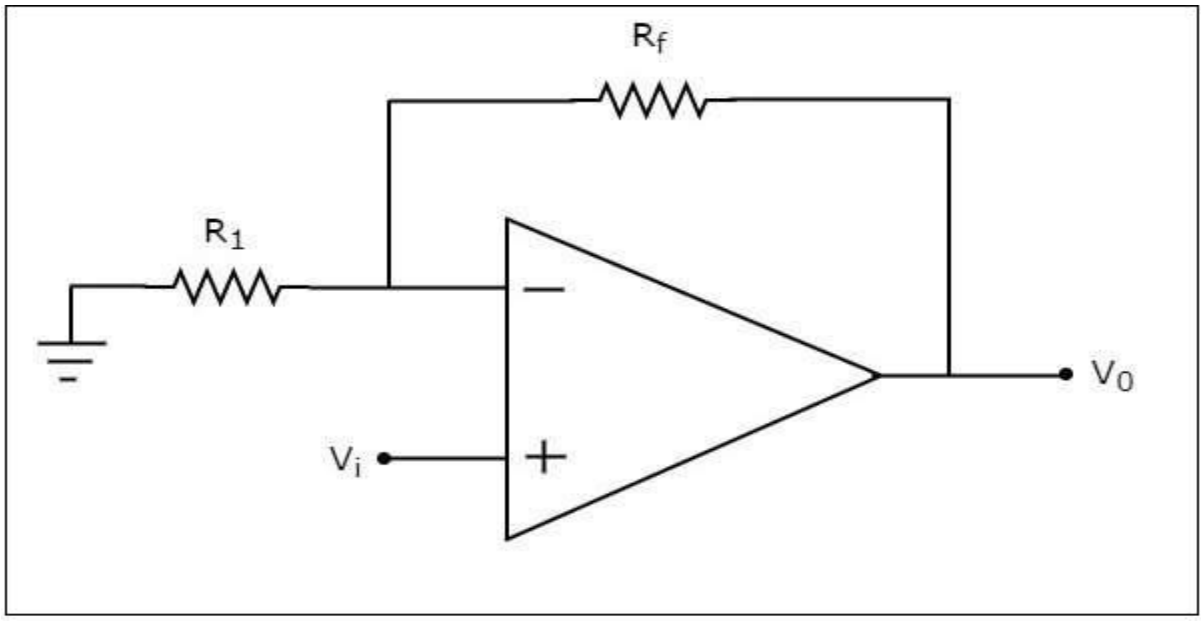
The ratio of the output voltage V0V0 and the input voltage ViVi is the voltage-gain or gain of the amplifier. Therefore, the **gain of inverting amplifier** is equal to −RfR1−RfR1.

Note that the gain of the inverting amplifier is having a **negative sign**. It indicates that there exists a 180^0 phase difference between the input and the output.

Non-Inverting Amplifier

A non-inverting amplifier takes the input through its non-inverting terminal, and produces its amplified version as the output. As the name suggests, this amplifier just amplifies the input, without inverting or changing the sign of the output.

The **circuit diagram** of a non-inverting amplifier is shown in the following figure −



In the above circuit, the input voltage ViVi is directly applied to the non-inverting input terminal of op-amp. So, the voltage at the non-inverting input terminal of the op-amp will be ViVi.

By using **voltage division principle**, we can calculate the voltage at the inverting input terminal of the op-amp as shown below −

$$=>V1=V0(R1R1+Rf)=>V1=V0(R1R1+Rf)$$

According to the **virtual short concept**, the voltage at the inverting input terminal of an op-amp is same as that of the voltage at its non-inverting input terminal.

$$=>V1=Vi=>V1=Vi$$

$$=>V0(R1R1+Rf)=Vi=>V0(R1R1+Rf)=Vi$$

$$=>V0Vi=R1+RfR1=>V0Vi=R1+RfR1$$

$$=>V0Vi=1+RfR1=>V0Vi=1+RfR1$$

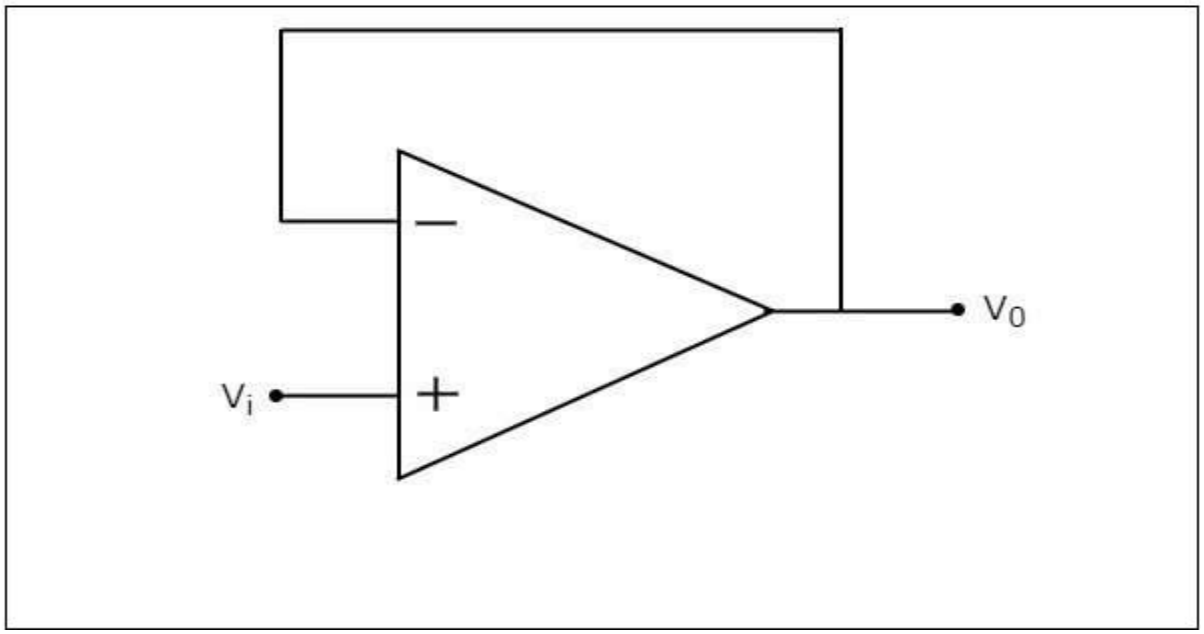
Now, the ratio of output voltage V0V0 and input voltage ViVi or the voltage-gain or **gain of the non-inverting amplifier** is equal to 1+RfR11+RfR1.

Note that the gain of the non-inverting amplifier is having a **positive sign**. It indicates that there is no phase difference between the input and the output.

Voltage follower

A **voltage follower** is an electronic circuit, which produces an output that follows the input voltage. It is a special case of non-inverting amplifier.

If we consider the value of feedback resistor, RfRf as zero ohms and (or) the value of resistor, 1 as infinity ohms, then a non-inverting amplifier becomes a voltage follower. The **circuit diagram** of a voltage follower is shown in the following figure −



In the above circuit, the input voltage ViVi is directly applied to the non-inverting input terminal of the op-amp. So, the voltage at the non-inverting input terminal of op-amp is equal to ViVi. Here, the output is directly connected to the inverting input terminal of opamp. Hence, the voltage at the inverting input terminal of op-amp is equal to V0V0.

According to the **virtual short concept**, the voltage at the inverting input terminal of the op-amp is same as that of the voltage at its non-inverting input terminal.

$$=>V0=Vi=>V0=Vi$$

So, the output voltage V0V0 of a voltage follower is equal to its input voltage ViVi.
Thus, the **gain of a voltage follower** is equal to one since, both output voltage V0V0 and input voltage ViVi of voltage follower are same.

Arithmetic Circuits

In the previous chapter, we discussed about the basic applications of op-amp. Note that they come under the linear operations of an op-amp. In this chapter, let us discuss about arithmetic circuits, which are also linear applications of op-amp.

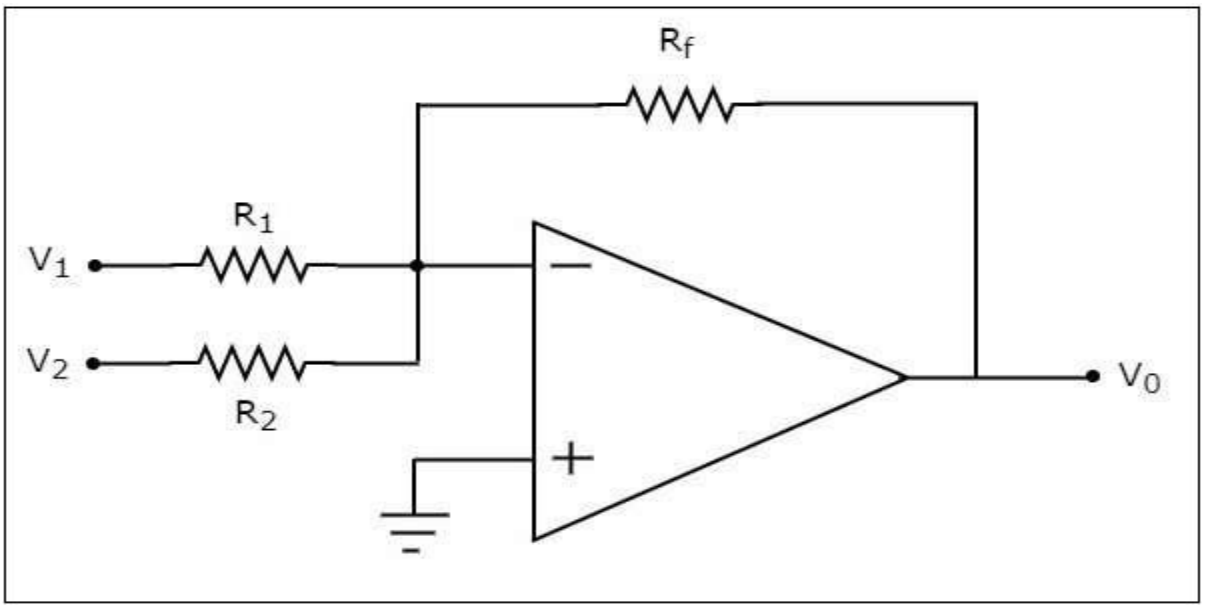
The electronic circuits, which perform arithmetic operations are called as **arithmetic circuits**. Using op-amps, you can build basic arithmetic circuits such as an **adder** and a **subtractor**. In this chapter, you will learn about each of them in detail.

Adder

An adder is an electronic circuit that produces an output, which is equal to the sum of the applied inputs. This section discusses about the op-amp based adder circuit.

An op-amp based adder produces an output equal to the sum of the input voltages applied at its inverting terminal. It is also called as a **summing amplifier**, since the output is an amplified one.

The **circuit diagram** of an op-amp based adder is shown in the following figure −



In the above circuit, the non-inverting input terminal of the op-amp is connected to ground. That means zero volts is applied at its non-inverting input terminal.

According to the **virtual short concept**, the voltage at the inverting input terminal of an op-amp is same as that of the voltage at its non-inverting input terminal. So, the voltage at the inverting input terminal of the op-amp will be zero volts.

The **nodal equation** at the inverting input terminal's node is

$$0−V1R1+0−V2R2+0−V0Rf=00−V1R1+0−V2R2+0−V0Rf=0$$

$$=>V1R1−V2R2=V0Rf=>V1R1−V2R2=V0Rf$$

$$=>V0=Rf(V1R1+V2R2)=>V0=Rf(V1R1+V2R2)$$

If Rf=R1=R2=RRf=R1=R2=R, then the output voltage V0V0 will be −

$$V0=−R(V1R+V2R)V0=−R(V1R+V2R)$$

$$=>V0=−(V1+V2)=>V0=−(V1+V2)$$

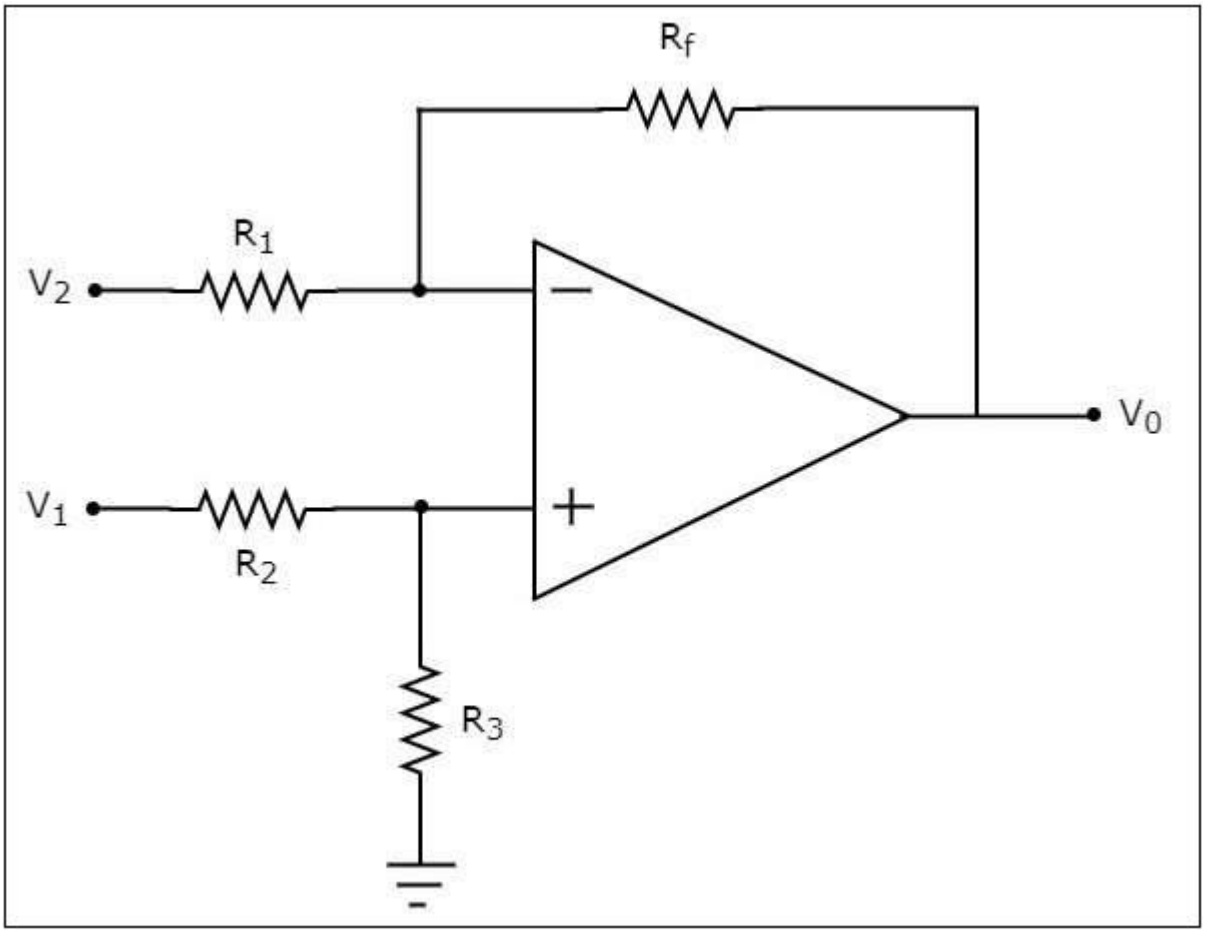
Therefore, the op-amp based adder circuit discussed above will produce the sum of the two input voltages v1v1 and v1v1, as the output, when all the resistors present in the circuit are of same value. Note that the output voltage V0V0 of an adder circuit is having a **negative sign**, which indicates that there exists a 180^0 phase difference between the input and the output.

Subtractor

A subtractor is an electronic circuit that produces an output, which is equal to the difference of the applied inputs. This section discusses about the op-amp based subtractor circuit.

An op-amp based subtractor produces an output equal to the difference of the input voltages applied at its inverting and non-inverting terminals. It is also called as a **difference amplifier**, since the output is an amplified one.

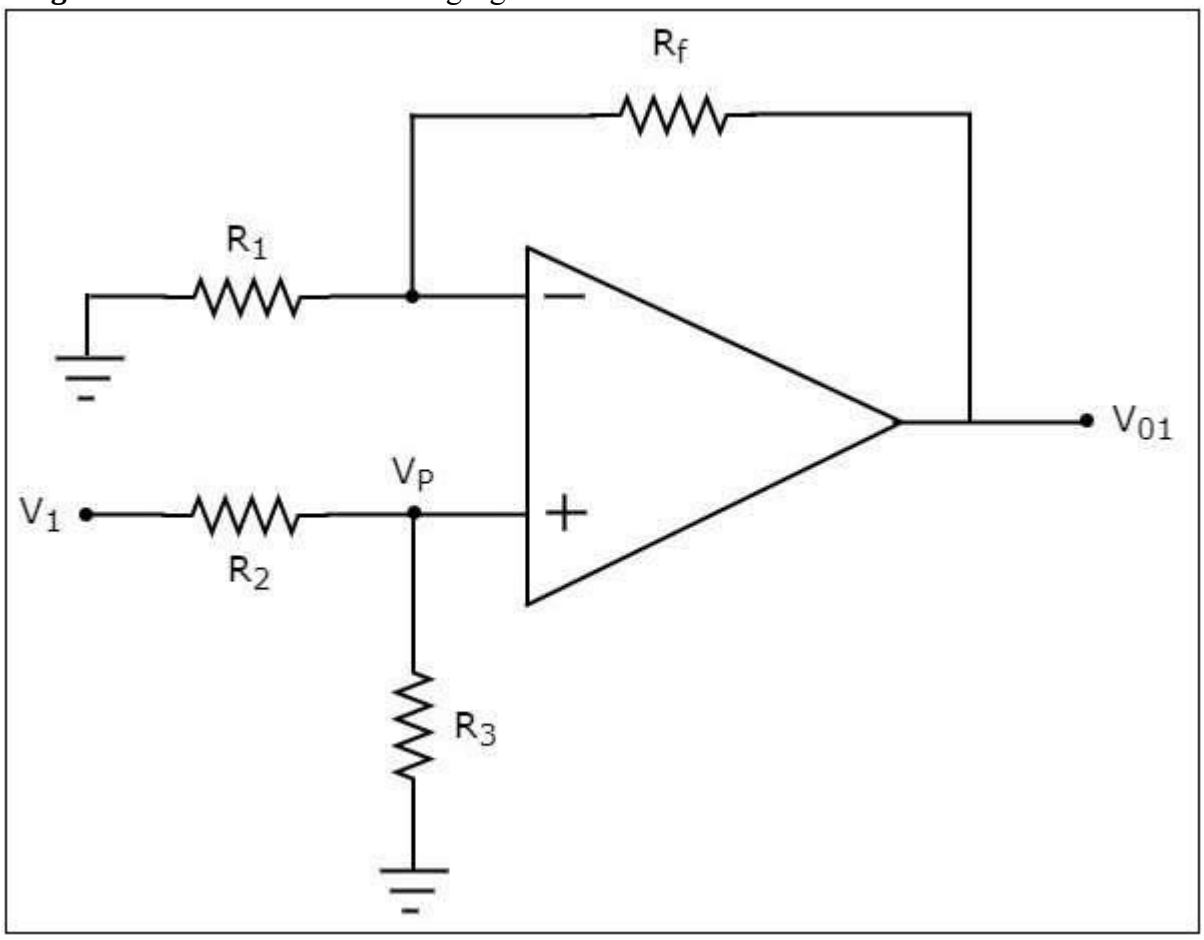
The **circuit diagram** of an op-amp based subtractor is shown in the following figure −



Now, let us find the expression for output voltage V0V0 of the above circuit using **superposition theorem** using the following steps −

Step 1

Firstly, let us calculate the output voltage V01V01 by considering only V1V1.
For this, eliminate V2V2 by making it short circuit. Then we obtain the **modified circuit diagram** as shown in the following figure −



Now, using the **voltage division principle**, calculate the voltage at the non-inverting input terminal of the op-amp.

$$=>Vp=V1(R3R2+R3)=>Vp=V1(R3R2+R3)$$

Now, the above circuit looks like a non-inverting amplifier having input voltage VpVp. Therefore, the output voltage V01V01 of above circuit will be

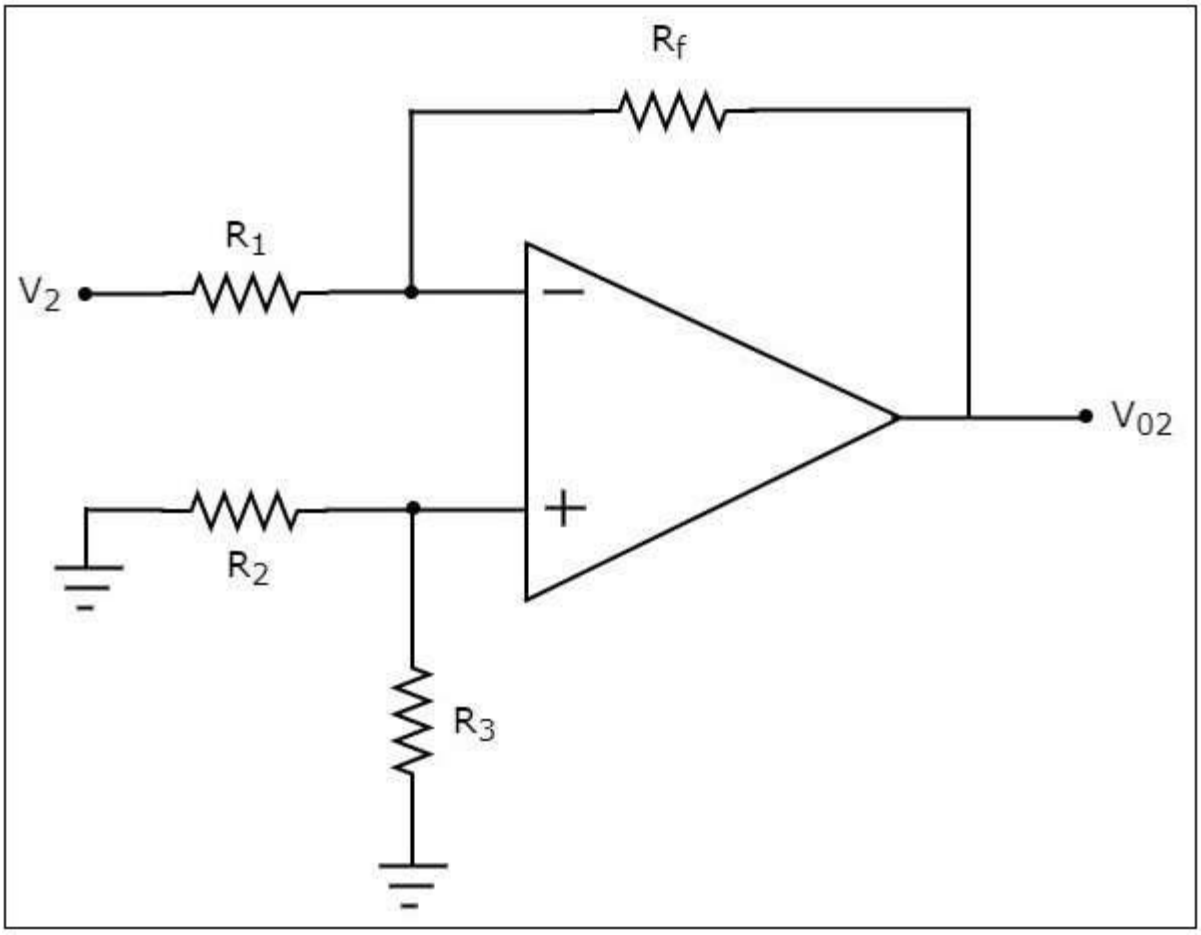
$$V01=Vp(1+RfR1)V01=Vp(1+RfR1)$$

Substitute, the value of VpVp in above equation, we obtain the output voltage V01V01 by considering only V1V1, as −

$$V01=V1(R3R2+R3)(1+RfR1)V01=V1(R3R2+R3)(1+RfR1)$$

Step 2

In this step, let us find the output voltage, V02V02 by considering only V2V2. Similar to that in the above step, eliminate V1V1 by making it short circuit. The **modified circuit diagram** is shown in the following figure.



You can observe that the voltage at the non-inverting input terminal of the op-amp will be zero volts. It means, the above circuit is simply an **inverting op-amp**. Therefore, the output voltage V02V02 of above circuit will be −

$$V02=(-RfR1)V2V02=(-RfR1)V2$$

Step 3

In this step, we will obtain the output voltage V0V0 of the subtractor circuit by **adding the output voltages** obtained in Step1 and Step2. Mathematically, it can be written as

$$V0=V01+V02V0=V01+V02$$

Substituting the values of V01V01 and V02V02 in the above equation, we get −

$$V0=V1(R3R2+R3)(1+RfR1)+(-RfR1)V2V0=V1(R3R2+R3)(1+RfR1)+(-RfR1)V2$$

$$=>V0=V1(R3R2+R3)(1+RfR1)-(RfR1)V2=>V0=V1(R3R2+R3)(1+RfR1)-(RfR1)V2$$

If Rf=R1=R2=R3=RRf=R1=R2=R3=R, then the output voltage V0V0 will be

$$V0=V1(RR+R)(1+RR)-(RR)V2V0=V1(RR+R)(1+RR)-(RR)V2$$

$$=>V0=V1(R2R)(2)-(1)V2=>V0=V1(R2R)(2)-(1)V2$$

$$V0=V1-V2V0=V1-V2$$

Thus, the op-amp based subtractor circuit discussed above will produce an output, which is the difference of two input voltages V1V1 and V2V2, when all the resistors present in the circuit are of same value.

Instrumentation Amplifier

Instrumentation Amplifiers are basically used to amplify small differential signals. Instrumentation Amplifier provides the most important function of Common-Mode Rejection (CMR). It cancels out any signals that have the same potential on both the inputs. The signals that have a potential difference between the inputs get amplified.

An Instrumentation Amplifier (In-Amp) is used for low-frequency signals (≪1 MHz) to provide a large amount of Gain. It amplifies the input signal rejecting Common-Mode Noise that is present in the input signal.

Basically, a typical Instrumentation Amplifier configuration consists of three Op-amps and several resistors. To achieve the highest CMRR (Common Mode Rejection Ratio), high-precision resistors are used (0.1 % tolerance or better).
Fig. 2 below shows the Pin configuration and Physical view of IC, AD620 In-Amp (Instrumentation Amplifier). This has been the industry standard, high performance, low cost amplifier. It is completely monolithic available in both 8-lead DIP and SOIC packages. The user can obtain any desired gain from 1 to 1000 using a single external resistor. By design, the fixed resistor values for gains of 10 and 100 are standard 1% metal film resistor values.

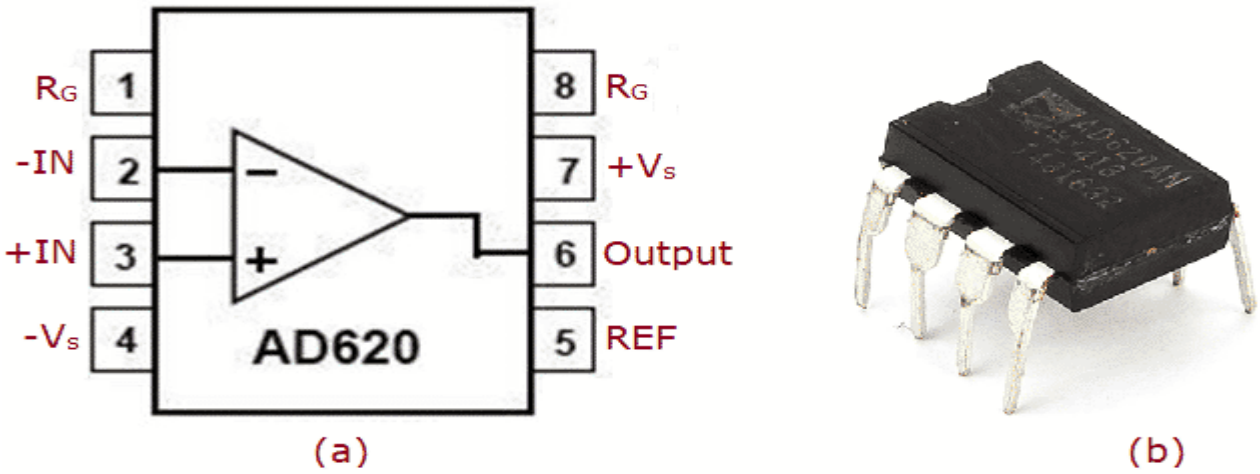


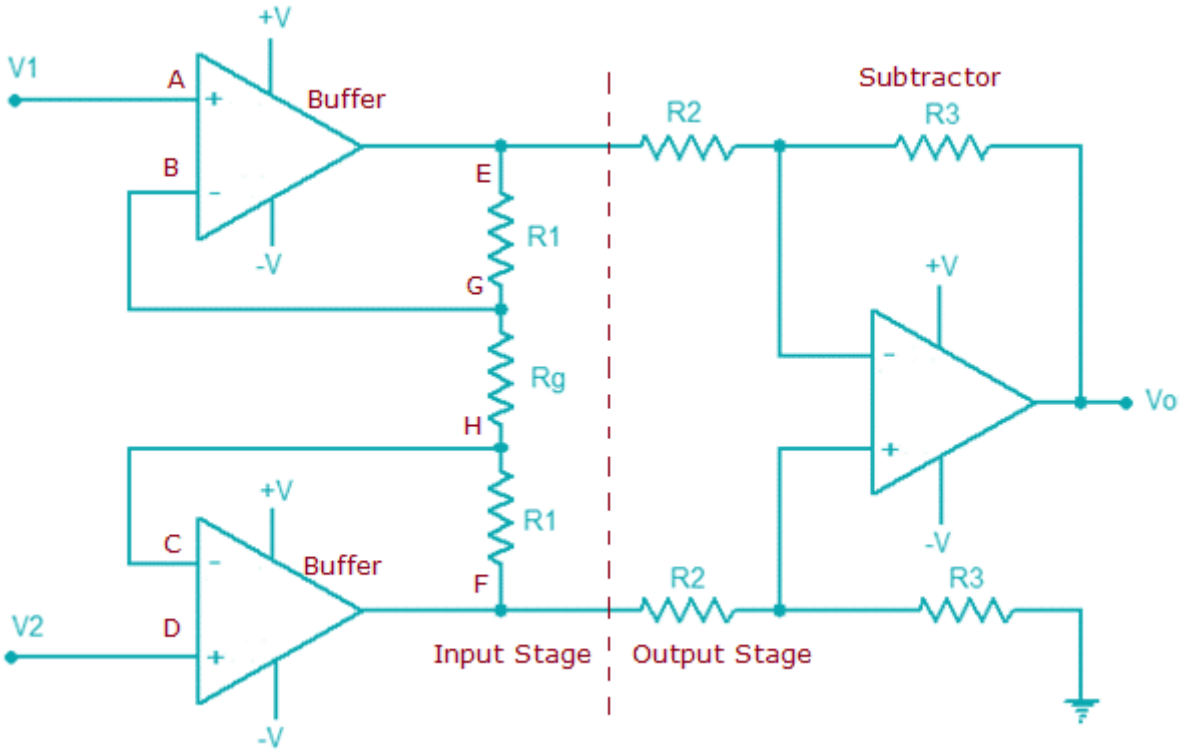
Fig. 2 – (a) Pin Configuration (b) AD620 Instrumentation Amplifier.

Working Principle of Instrumentation Amplifier

Figure 3 below represents the configuration of the Instrumentation Amplifier using two Op-amps where V1 and V2 are the input voltages and V01, Vo2 are the outputs of the Op-amp 1 and Op-amp 2 respectively. R1, R2, R3 are the resistors and the output stage of the Instrumentation Amplifier is a difference amplifier, whose output V_{out} is the amplified difference of the input signals.

The inputs of the two buffer Op-amps draw no current and hence the voltage drop across Rg is proportional to the differential voltage V1 and V2. This produces a current that runs entirely through the resistors R and the voltage produced acts as the input to the differential amplifier or Subtractor circuit

All the Resistors except Rg are equal. Rg may be an external resistor connected across two pins of the IC. If the pins are not connected, then the gain of the amplifier is 1 but preferably different gains may be obtained by connecting a resistor of relevant value. Alternatively, a number of resistors may be fabricated on the chip to give Gains of 1, 10, 100 and 1000.



Instrumentation Amplifier Configuration

Similar to the Op-amp circuit, the input buffer amplifiers (Op-amp 1 and Op-amp 2) of the Instrumentation Amplifier pass the common-mode signal through at unity gain. The signal gets amplified by both buffers. The output signals from the two buffers connect to the subtractor section of the Instrumentation amplifier. The differential signal is amplified at low gain or unity and the common-mode voltage is attenuated.

The potential at node A is the inverting input voltage V_1. From the virtual short concept the potential at node B and G is also V_1. The potential at node D is the non-inverting input voltage V_2. Hence the potential at node C and H is also V_2 .

The current I through the resistors R_1, R_{gain} and R_1 remains the same as ideally the current to the input stage Op-amps is zero.

Applying Ohm's law between the nodes E and F

$I = (V_{o1}-V_{o2})/(R_1+R_{gain}+R_1)$

$I = (V_{o1}-V_{o2})/(2R_1+R_{gain})$

Since there is no current flow to the input of the op-amps 1 & 2, the current I between the nodes G and H can be given as,

$I = (V_G-V_H)/R_{gain} = (V_1-V_2)/R_{gain}$

The output of the difference amplifier is given by: –

$\mathbf{V_o = (R_3/R_2)(V_{o1}-V_{o2})}$

Theoretically, this means that the end user may obtain Gain in the front end as desired without increasing the common-mode gain and error. That is, the differential signal will be increased by gain and thus CMRR is directly proportional to gain.

Applications of Instrumentation Amplifier

The applications of Instrumentation Amplifier are:

- They are used extensively in Bio-medical applications like ECG's and EEG's.
- Instrumentation Amplifiers are used where long-term stability is essential like Industrial applications that includes automation.
- Instrumentation amplifiers are incorporated with pressure transducers in Weighing Systems to monitor various physical quantities such as weight, force, pressure, displacement and torque.
- They are used in Gaming industry.
- Instrumentation Amplifiers are also used in hand held batteries.

Advantages of Instrumentation Amplifier

The advantages of Instrumentation Amplifier are:

- Offset voltage is minimized.
- Voltage Gain is high as the configuration uses high precision resistors.
- The Gain of the circuit can be varied by using specific value of resistor.
- Non-linearity is very low. It is an inherent performance limitation of the device and cannot be removed by external adjustment but can only be designed by the manufacturer.
- Input impedance is very high to avoid loading down the input signal source and Output impedance is very low.
- Common-mode rejection is very high.

Disadvantage of Instrumentation Amplifier

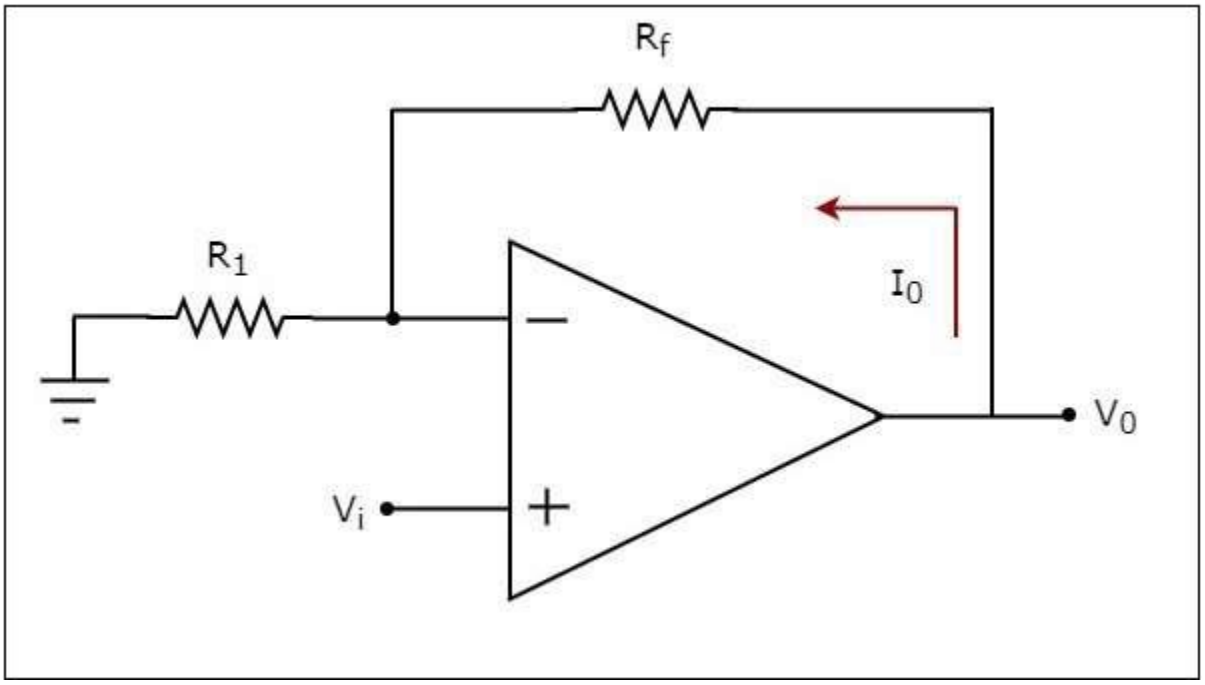
The biggest disadvantage of Instrumentation Amplifier is the occurrence of noise when used for long range transmission purpose.

Voltage and current are the basic electrical quantities. They can be converted into one another depending on the requirement. **Voltage to Current Converter** and Current to **Voltage Converter** are the two circuits that help in such conversion. These are also linear applications of op-amps. This chapter discusses them in detail.

Voltage to Current Converter

A **voltage to current converter** or **V to I converter**, is an electronic circuit that takes current as the input and produces voltage as the output. This section discusses about the op-amp based voltage to current converter.

An op-amp based voltage to current converter produces an output current when a voltage is applied to its non-inverting terminal. The **circuit diagram** of an op-amp based voltage to current converter is shown in the following figure.



In the circuit shown above, an input voltage ViVi is applied at the non-inverting input terminal of the op-amp. According to the **virtual short concept**, the voltage at the inverting input terminal of an op-amp will be equal to the voltage at its non-inverting input terminal . So, the voltage at the inverting input terminal of the op-amp will be ViVi.

The **nodal equation** at the inverting input terminal's node is −

ViR1−I0=0ViR1−I0=0

=>I0=VtR1=>I0=VtR1

Thus, the **output current** I0I0 of a voltage to current converter is the ratio of its input voltage ViVi and resistance R1R1.

We can re-write the above equation as −

I0Vi=1R1I0Vi=1R1

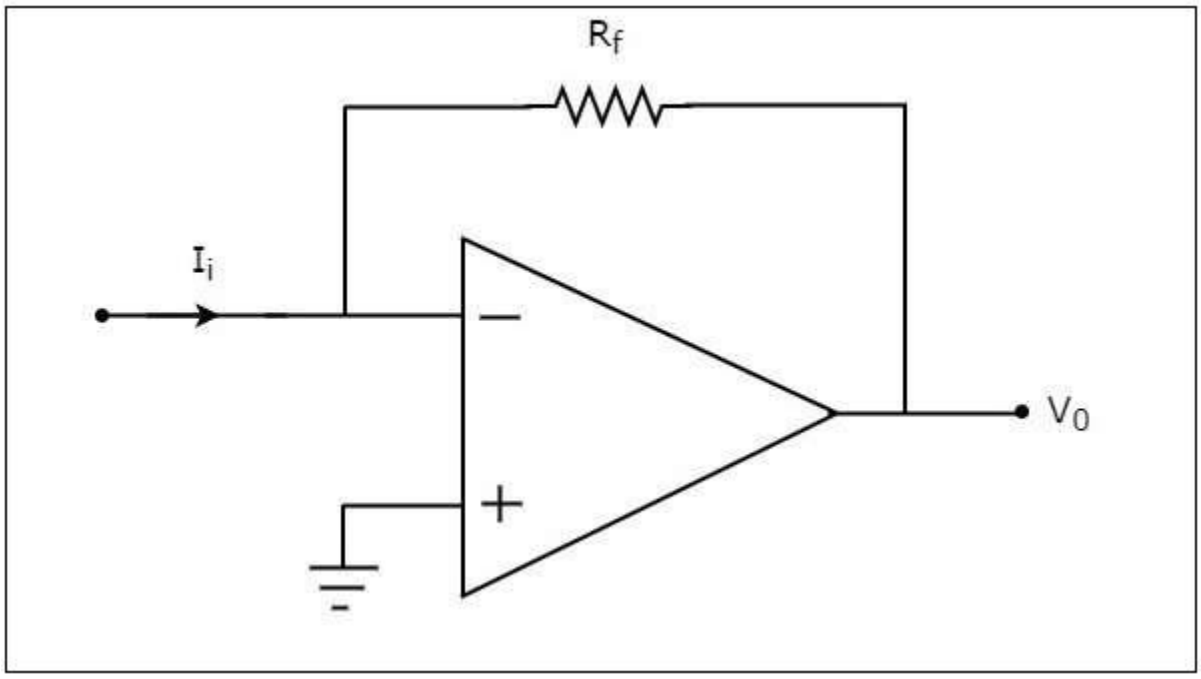
The above equation represents the ratio of the output current I0I0 and the input voltage ViVi & it is equal to the reciprocal of resistance R1R1 The ratio of the output current I0I0 and the input voltage ViVi is called as **Transconductance**.

We know that the ratio of the output and the input of a circuit is called as gain. So, the gain of an voltage to current converter is the Transconductance and it is equal to the reciprocal of resistance R1R1.

Current to Voltage Converter

A **current to voltage converter** or **I to V converter** is an electronic circuit that takes current as the input and produces voltage as the output. This section discusses about the op-amp based current to voltage converter.

An op-amp based current to voltage converter produces an output voltage when current is applied to its inverting terminal. The **circuit diagram** of an op-amp based current to voltage converter is shown in the following figure.



In the circuit shown above, the non-inverting input terminal of the op-amp is connected to ground. That means zero volts is applied at its non-inverting input terminal.

According to the **virtual short concept**, the voltage at the inverting input terminal of an op-amp will be equal to the voltage at its non-inverting input terminal. So, the voltage at the inverting input terminal of the op-amp will be zero volts.

The **nodal equation** at the inverting terminal's node is −

$$-Ii+0-V0Rf=0-Ii+0-V0Rf=0$$

$$-Ii=V0Rf-Ii=V0Rf$$

$$V0=-RtIiV0=-RtIi$$

Thus, the **output voltage,** V0V0 of current to voltage converter is the (negative) product of the feedback resistance, RfRf and the input current, ItIt. Observe that the output voltage, V0V0 is having a **negative sign**, which indicates that there exists a 180^0 phase difference between the input current and output voltage.

We can re-write the above equation as −

$$V0Ii=-RfV0Ii=-Rf$$

Sample and hold circuit using op-amp

As the name indicates , a sample and hold circuit is a circuit which samples an input signal and holds onto its last sampled value until the input is sampled again. Sample and hold circuits are commonly used in analogue to digital converts, communication circuits, PWM circuits etc. The circuit shown below is of a sample and hold circuit based on uA 741 opamp , n-channel E MOSFET BS170 and few passive components. So let's begin to learn in detail about creating a sample and hold circuit.

Description

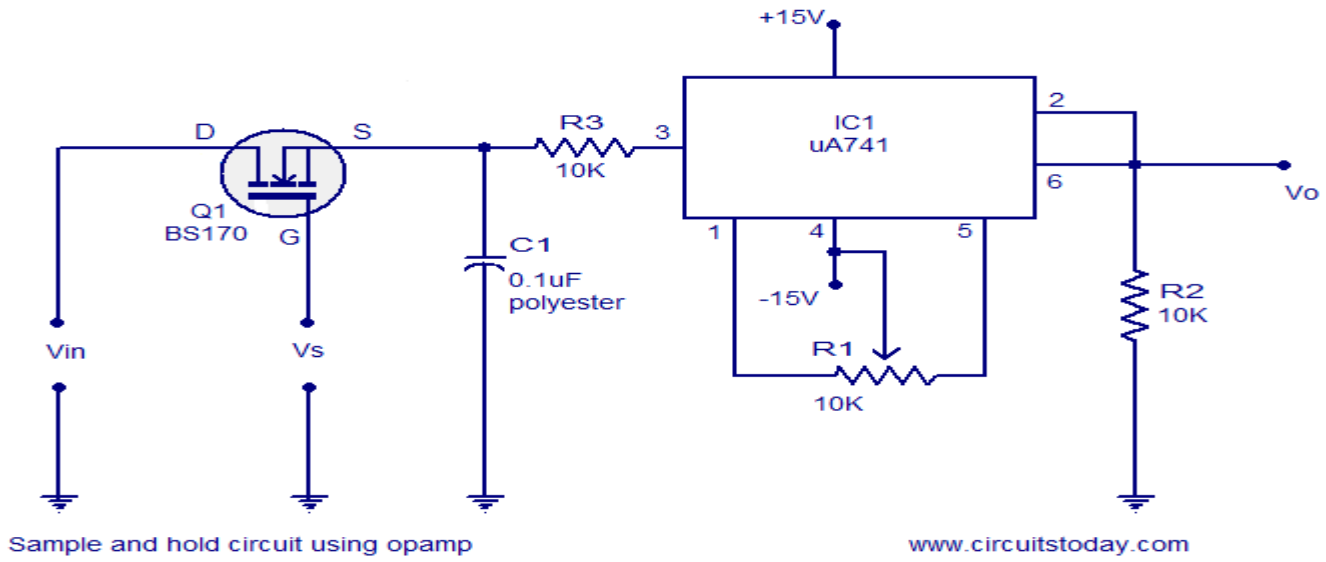
As the name indicates , a sample and hold circuit is a circuit which samples an input signal and holds onto its last sampled value until the input is sampled again. Sample and hold circuits are commonly used in analogue to digital converts, communication circuits, PWM circuits etc. The circuit shown below is of a sample and hold circuit based on uA 741 opamp , n-channel E MOSFET BS170 and few passive components.

In the circuit MOSFET BS170 (Q1) works as a switch while opamp uA741 is wired as a voltage follower. The signal to be sampled (Vin) is applied to the drain of MOSFET while the sample and hold control voltage (Vs) is applied to the source of the MOSFET. The source pin of the MOSFET is connected to the non inverting input of the opamp through the resistor R3. C1 which is a polyester capacitor serves as the charge storing device. Resistor R2 serves as the load resistor while preset R1 is used for adjusting the offset voltage.

During the positive half cycle of the Vs, the MOSFET is ON which acts like a closed switch and the capacitor C1 is charged by the Vin and the same voltage (Vin) appears at the output of the opamp. When Vs is zero MOSFET is switched off and the only discharge path for C1 is through the inverting input of the opamp. Since the input impedance of the opamp is too high the voltage Vin is retained and it appears at the output of the opamp.

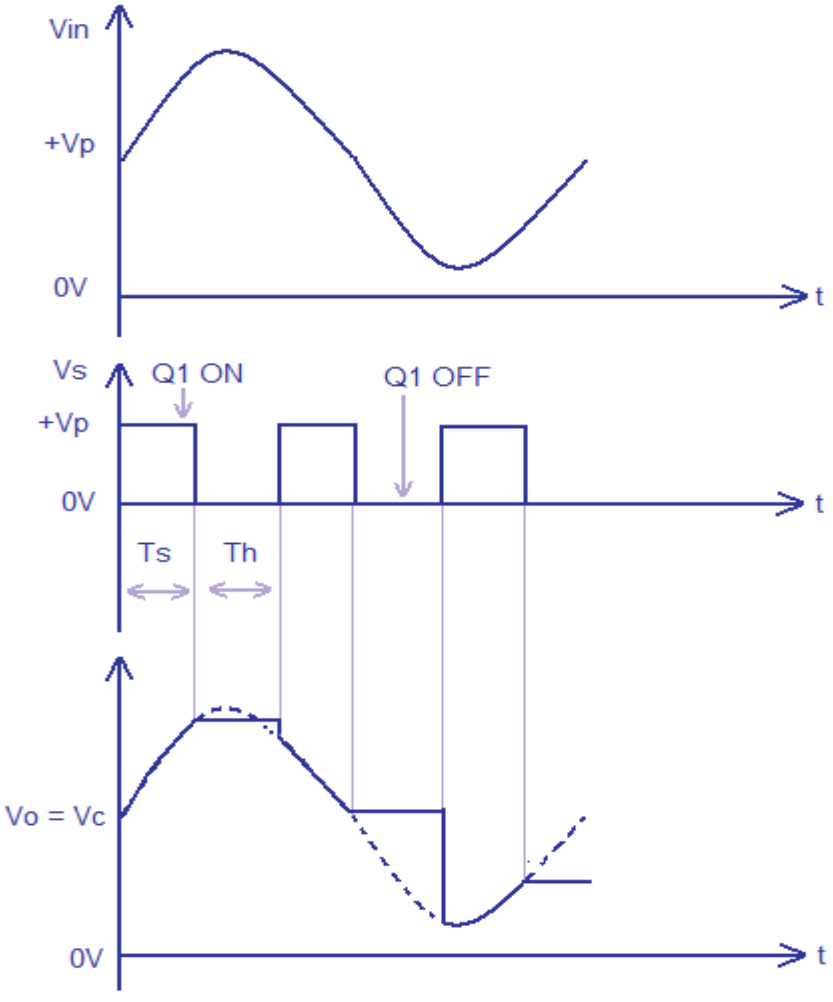
The time periods of the Vs during which the voltage across the capacitor (Vc) is equal to Vin are called sample periods (Ts) and the time periods of Vs during which the voltage across the capacitor C1 (Vc) is held constant are called hold periods (Th). Taking a close look at the input and output wave forms of the circuit will make it easier to understand the working of the circuit.

Circuit diagram



Sample and Hold circuit using uA741 opamp

Input and output waveforms.



input and output waveforms

Input and output waveforms – Sample and hold circuit

Differentiator And Integrator

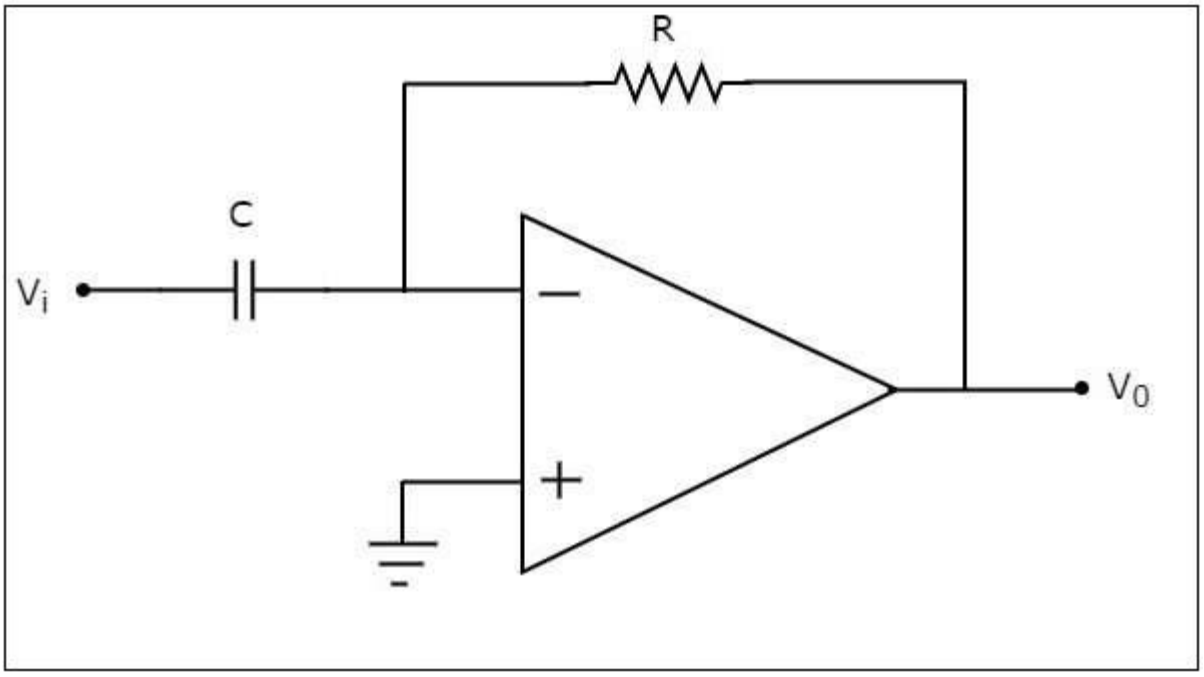
The electronic circuits which perform the mathematical operations such as differentiation and integration are called as differentiator and integrator, respectively.

This chapter discusses in detail about op-amp based **differentiator** and integrator. Please note that these also come under linear applications of op-amp.

Differentiator

A **differentiator** is an electronic circuit that produces an output equal to the first derivative of its input. This section discusses about the op-amp based differentiator in detail.

An op-amp based differentiator produces an output, which is equal to the differential of input voltage that is applied to its inverting terminal. The **circuit diagram** of an op-amp based differentiator is shown in the following figure –



In the above circuit, the non-inverting input terminal of the op-amp is connected to ground. That means zero volts is applied to its non-inverting input terminal.

According to the **virtual short concept**, the voltage at the inverting input terminal of opamp will be equal to the voltage present at its non-inverting input terminal. So, the voltage at the inverting input terminal of op-amp will be zero volts.

The nodal equation at the inverting input terminal's node is −

$$Cd(0-Vi)dt+0-V0R=0Cd(0-Vi)dt+0-V0R=0$$

$$=>-CdVidt=V0R=>-CdVidt=V0R$$

$$=>V0=-RCdVidt=>V0=-RCdVidt$$

If RC=1secRC=1sec, then the output voltage V0V0 will be −

$$V0=-dVidtV0=-dVidt$$

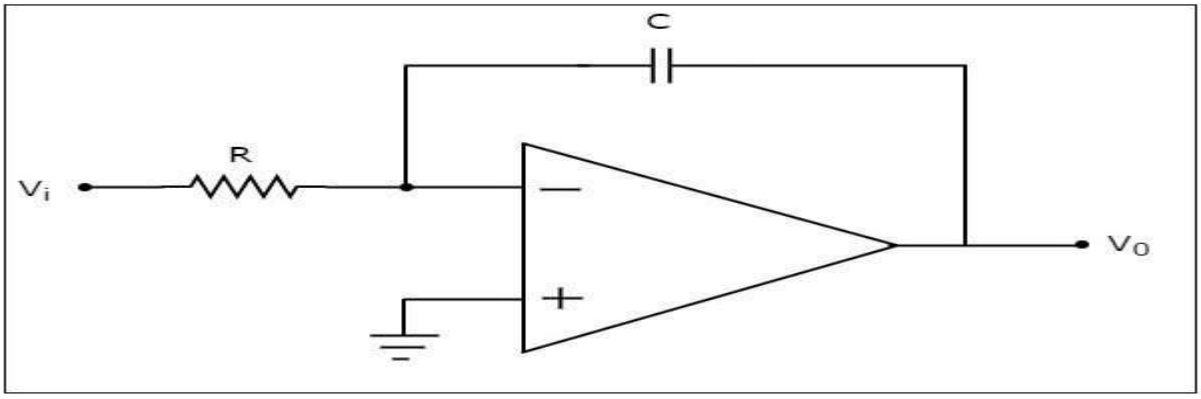
Thus, the op-amp based differentiator circuit shown above will produce an output, which is the differential of input voltage ViVi, when the magnitudes of impedances of resistor and capacitor are reciprocal to each other.

Note that the output voltage V0V0 is having a **negative sign**, which indicates that there exists a 180^0 phase difference between the input and the output.

Integrator

An **integrator** is an electronic circuit that produces an output that is the integration of the applied input. This section discusses about the op-amp based integrator.

An op-amp based integrator produces an output, which is an integral of the input voltage applied to its inverting terminal. The **circuit diagram** of an op-amp based integrator is shown in the following figure −



In the circuit shown above, the non-inverting input terminal of the op-amp is connected to ground. That means zero volts is applied to its non-inverting input terminal.

According to **virtual short concept**, the voltage at the inverting input terminal of op-amp will be equal to the voltage present at its non-inverting input terminal. So, the voltage at the inverting input terminal of op-amp will be zero volts.

The **nodal equation** at the inverting input terminal is −

$$0−ViR+Cd(0−V0)dt=00−ViR+Cd(0−V0)dt=0$$

$$=>−ViR=CdV0dt=>−ViR=CdV0dt$$

$$=>dV0dt=−ViRC=>dV0dt=−ViRC$$

$$=>dV0=(−ViRC)dt=>dV0=(−ViRC)dt$$

Integrating both sides of the equation shown above, we get −

$$∫dV0=∫(−ViRC)dt∫dV0=∫(−ViRC)dt$$

$$=>V0=−1RC∫Vtdt=>V0=−1RC∫Vtdt$$

If RC=1secRC=1sec, then the output voltage, V0V0 will be −

$$V0=−∫VidtV0=−∫Vidt$$

So, the op-amp based integrator circuit discussed above will produce an output, which is the integral of input voltage ViVi, when the magnitude of impedances of resistor and capacitor are reciprocal to each other.

Note − The output voltage, V0V0 is having a **negative sign**, which indicates that there exists 180^0 phase difference between the input and the output.

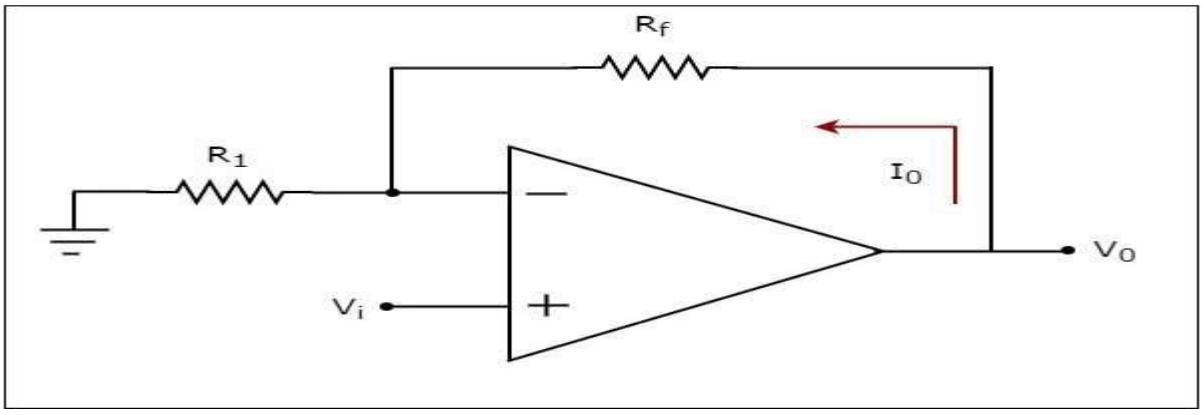
Converters Of Electrical Quantities

Voltage and current are the basic electrical quantities. They can be converted into one another depending on the requirement. **Voltage to Current Converter** and Current to **Voltage Converter** are the two circuits that help in such conversion. These are also linear applications of op-amps. This chapter discusses them in detail.

Voltage to Current Converter

A **voltage to current converter** or **V to I converter**, is an electronic circuit that takes current as the input and produces voltage as the output. This section discusses about the op-amp based voltage to current converter.

An op-amp based voltage to current converter produces an output current when a voltage is applied to its non-inverting terminal. The **circuit diagram** of an op-amp based voltage to current converter is shown in the following figure.



In the circuit shown above, an input voltage ViVi is applied at the non-inverting input terminal of the op-amp. According to the **virtual short concept**, the voltage at the inverting input terminal of an op-amp will be equal to the voltage at its non-inverting input terminal . So, the voltage at the inverting input terminal of the op-amp will be ViVi.

The **nodal equation** at the inverting input terminal's node is −

$$ViR1−I0=0ViR1−I0=0$$

$$=>I0=VtR1=>I0=VtR1$$

Thus, the **output current** I0I0 of a voltage to current converter is the ratio of its input voltage ViVi and resistance R1R1.

We can re-write the above equation as −

$$I0Vi=1R1I0Vi=1R1$$

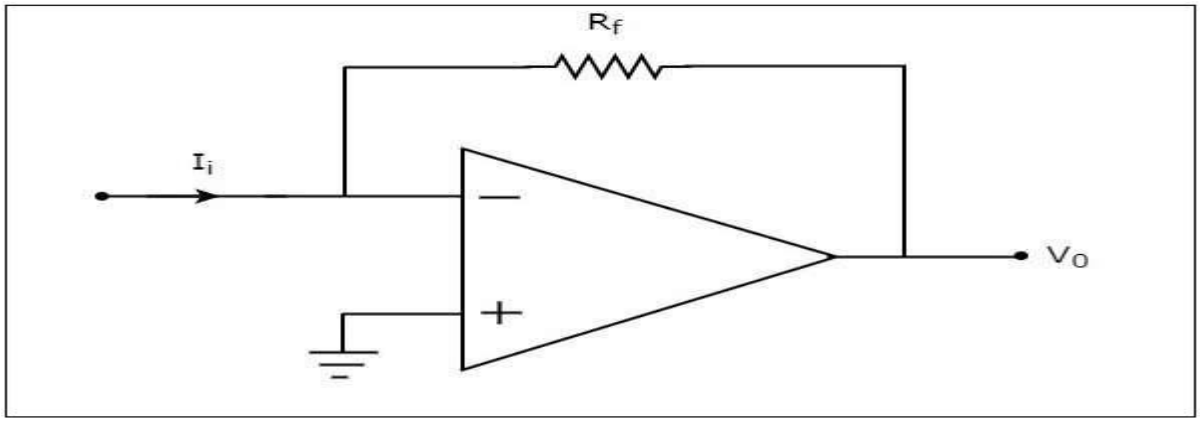
The above equation represents the ratio of the output current I0I0 and the input voltage ViVi & it is equal to the reciprocal of resistance R1R1 The ratio of the output current I0I0 and the input voltage ViVi is called as **Transconductance**.

We know that the ratio of the output and the input of a circuit is called as gain. So, the gain of an voltage to current converter is the Transconductance and it is equal to the reciprocal of resistance R1R1.

Current to Voltage Converter

A **current to voltage converter** or **I to V converter** is an electronic circuit that takes current as the input and produces voltage as the output. This section discusses about the op-amp based current to voltage converter.

An op-amp based current to voltage converter produces an output voltage when current is applied to its inverting terminal. The **circuit diagram** of an op-amp based current to voltage converter is shown in the following figure.



In the circuit shown above, the non-inverting input terminal of the op-amp is connected to ground. That means zero volts is applied at its non-inverting input terminal.

According to the **virtual short concept**, the voltage at the inverting input terminal of an op-amp will be equal to the voltage at its non-inverting input terminal. So, the voltage at the inverting input terminal of the op-amp will be zero volts.

The **nodal equation** at the inverting terminal's node is −

$$-Ii+0-V0Rf=0-Ii+0-V0Rf=0$$

$$-Ii=V0Rf-Ii=V0Rf$$

$$V0=-RtIiV0=-RtIi$$

Thus, the **output voltage,** V0 of current to voltage converter is the (negative) product of the feedback resistance, Rf and the input current, It. Observe that the output voltage, V0 is having a **negative sign**, which indicates that there exists a 180^0 phase difference between the input current and output voltage.

We can re-write the above equation as −

$$V0Ii=-RfV0Ii=-Rf$$

The above equation represents the ratio of the output voltage V0V0 and the input current IiIi, and it is equal to the negative of feedback resistance, RfRf. The ratio of output voltage V0V0 and input current IiIi is called as **Transresistance**.
We know that the ratio of output and input of a circuit is called as **gain**. So, the gain of a current to voltage converter is its trans resistance and it is equal to the (negative) feedback resistance RfRf .

Comparators

A **comparator** is an electronic circuit, which compares the two inputs that are applied to it and produces an output. The output value of the comparator indicates which of the inputs is greater or lesser. Please note that comparator falls under non-linear applications of ICs.

An op-amp consists of two input terminals and hence an op-amp based comparator compares the two inputs that are applied to it and produces the result of comparison as the output. This chapter discusses about **op-amp based comparators**.

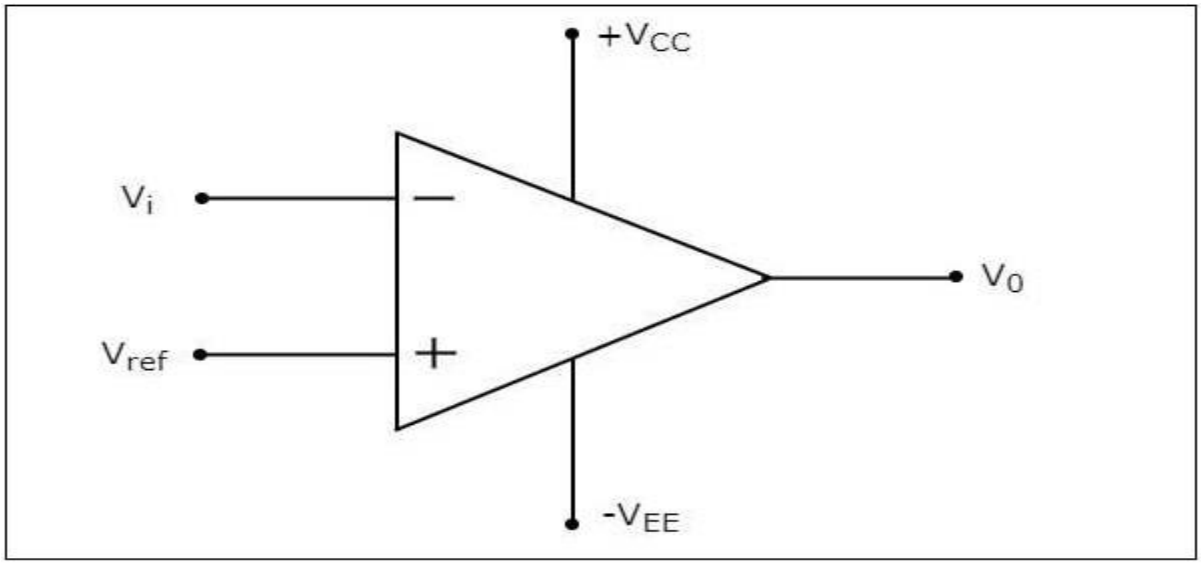
Types of Comparators

Comparators are of two types : **Inverting** and **Non-inverting**. This section discusses about these two types in detail.

Inverting Comparator

An **inverting comparator** is an op-amp based comparator for which a reference voltage is applied to its non-inverting terminal and the input voltage is applied to its inverting terminal. This comparator is called as **inverting** comparator because the input voltage, which has to be compared is applied to the inverting terminal of op-amp.

The **circuit diagram** of an inverting comparator is shown in the following figure.

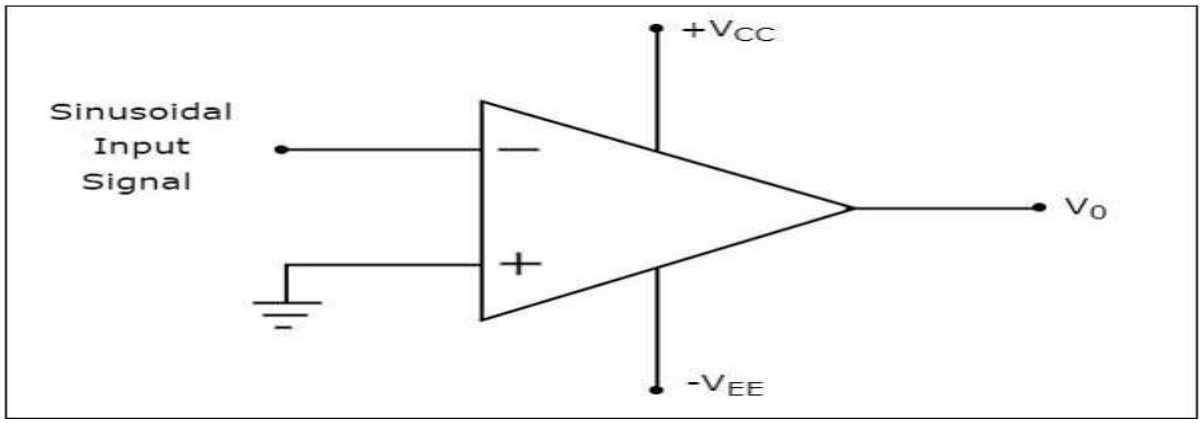


The **operation** of an inverting comparator is very simple. It produces one of the two values, +Vsat+Vsat and −Vsat−Vsat at the output based on the values of its input voltage ViVi and the reference voltage VrefVref.

- The output value of an inverting comparator will be −Vsat−Vsat, for which the input ViVi voltage is greater than the reference voltage VrefVref.
- The output value of an inverting comparator will be +Vsat+Vsat, for which the input ViVi is less than the reference voltage VrefVref.

Example

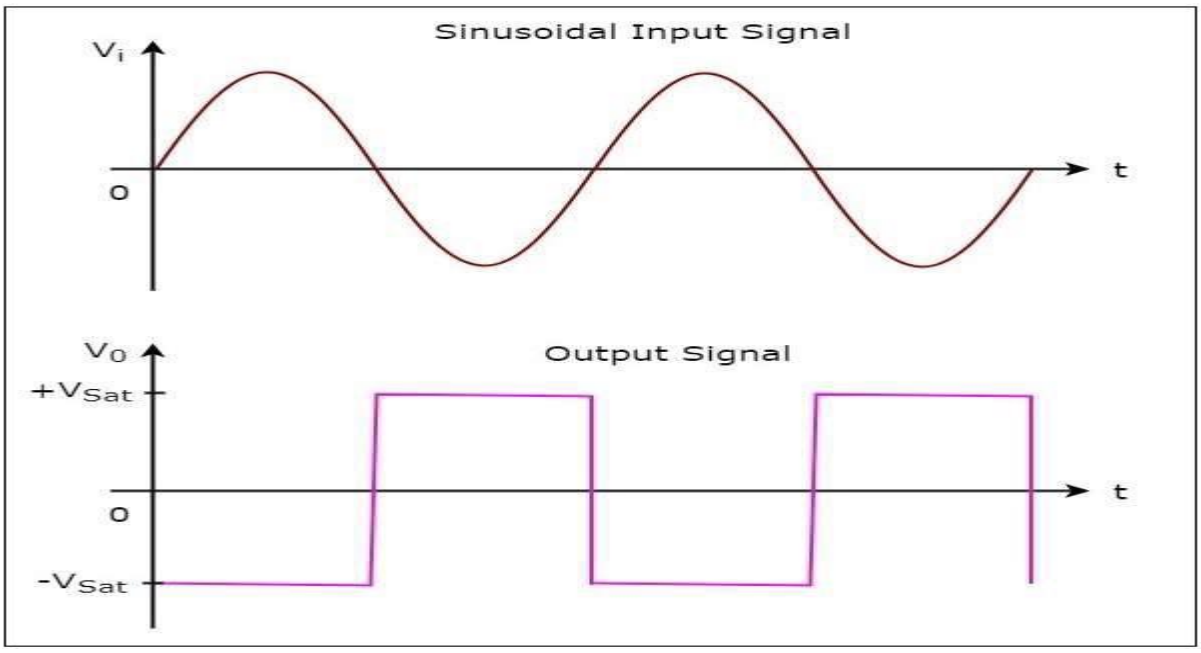
Let us draw the **output wave form** of an inverting comparator, when a sinusoidal input signal and a reference voltage of zero volts are applied to its inverting and non-inverting terminals respectively.



The **operation** of the inverting comparator shown above is discussed below −

- During the **positive half cycle** of the sinusoidal input signal, the voltage present at the inverting terminal of op-amp is greater than zero volts. Hence, the output value of the inverting comparator will be equal to −Vsat−Vsat during positive half cycle of the sinusoidal input signal.
- Similarly, during the **negative half cycle** of the sinusoidal input signal, the voltage present at the inverting terminal of the op-amp is less than zero volts. Hence, the output value of the inverting comparator will be equal to +Vsat+Vsat during negative half cycle of the sinusoidal input signal.

The following figure shows the **input and output waveforms** of an inverting comparator, when the reference voltage is zero volts.

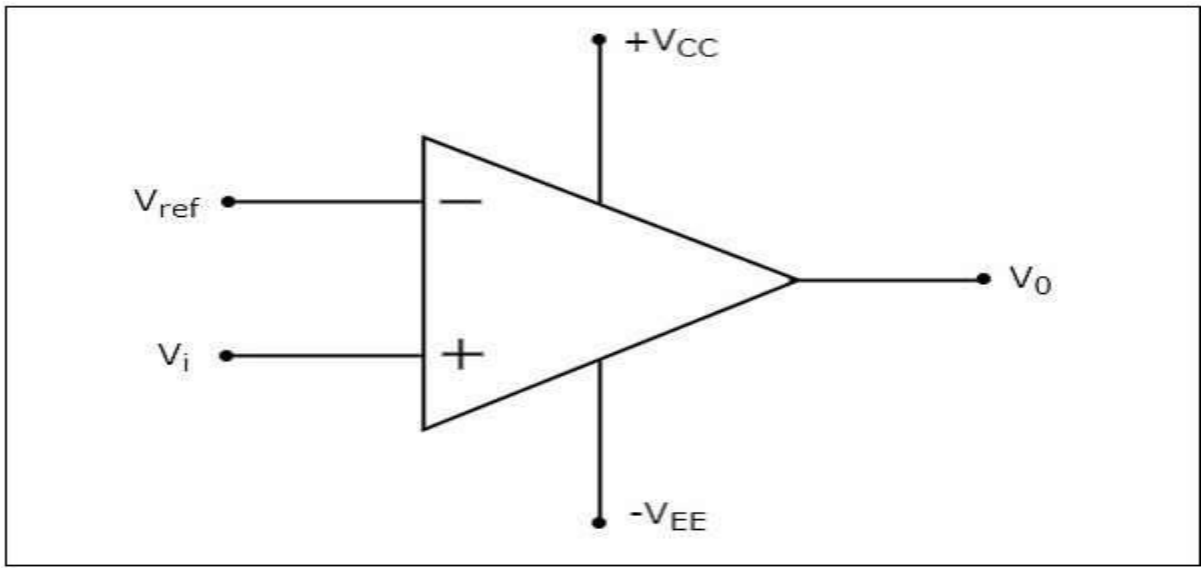


In the figure shown above, we can observe that the output transitions either from −Vsat−Vsat to +Vsat+Vsat or from +Vsat+Vsat to −Vsat−Vsat whenever the sinusoidal input signal is crossing zero volts. In other words, output changes its value when the input is crossing zero volts. Hence, the above circuit is also called as **inverting zero crossing detector.**

Non-Inverting Comparator

A non-inverting comparator is an op-amp based comparator for which a reference voltage is applied to its inverting terminal and the input voltage is applied to its non-inverting terminal. This op-amp based comparator is called as **non-inverting** comparator because the input voltage, which has to be compared is applied to the non-inverting terminal of the op-amp.

The **circuit diagram** of a non-inverting comparator is shown in the following figure

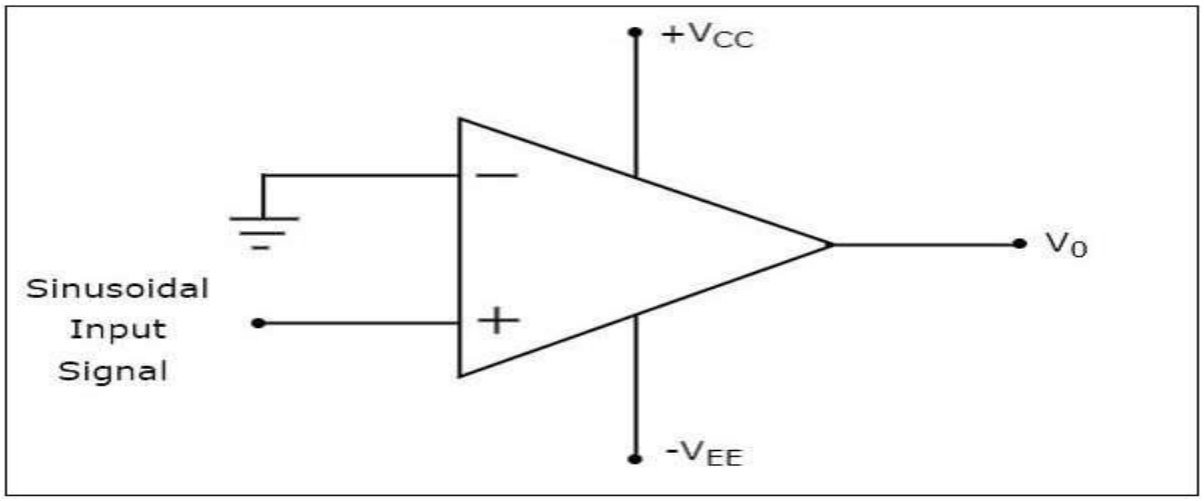


The **operation** of a non-inverting comparator is very simple. It produces one of the two values, +Vsat+Vsat and −Vsat−Vsat at the output based on the values of input voltage VtVt and the reference voltage +Vref+Vref.

- The output value of a non-inverting comparator will be +Vsat+Vsat, for which the input voltage ViVi is greater than the reference voltage +Vref+Vref.
- The output value of a non-inverting comparator will bee −Vsat−Vsat, for which the input voltage ViVi is less than the reference voltage +Vref+Vref.

Example

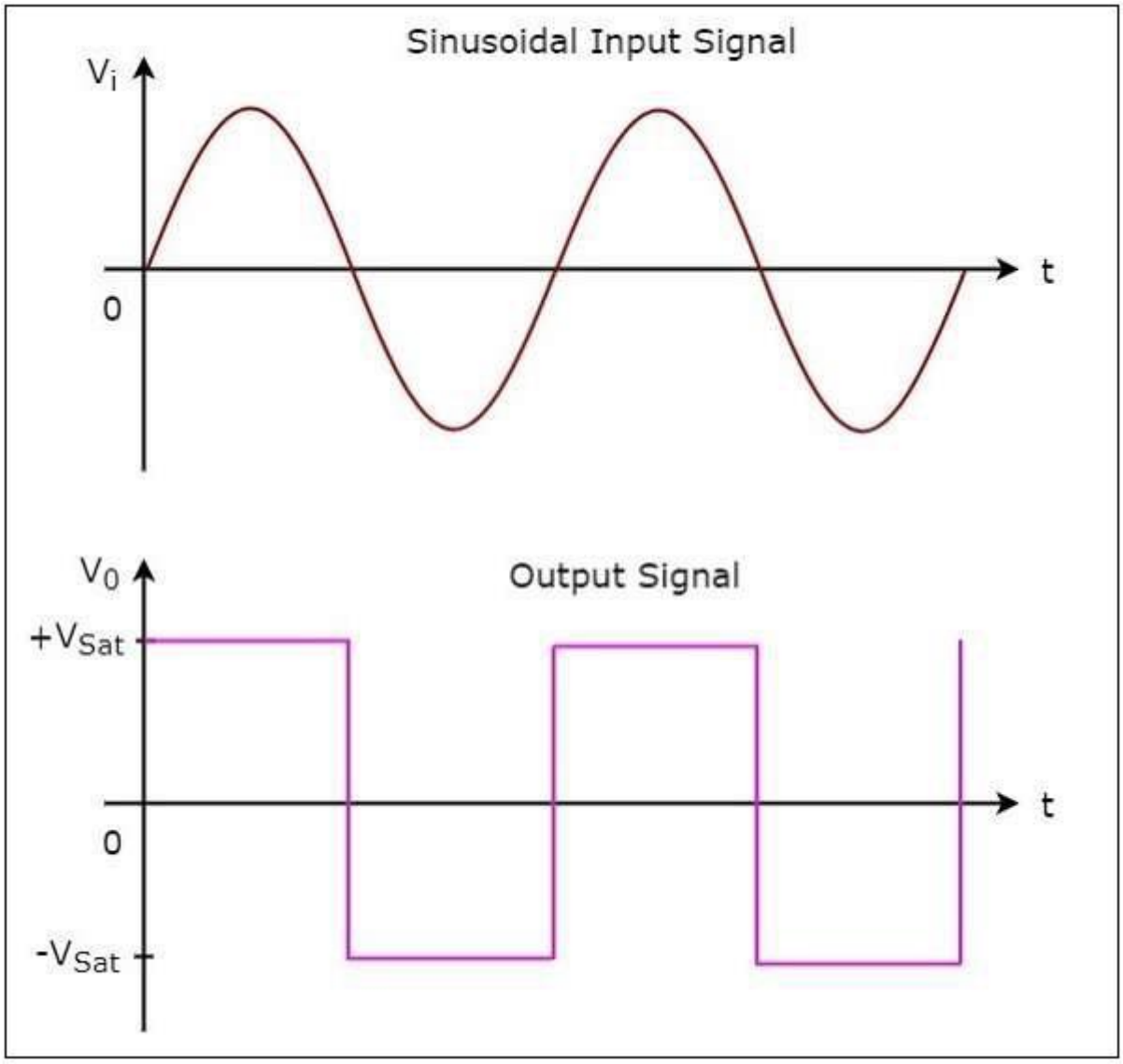
Let us draw the **output wave form** of a non-inverting comparator, when a sinusoidal input signal and reference voltage of zero volts are applied to the non-inverting and inverting terminals of the op-amp respectively.



The **operation** of a non-inverting comparator is explained below –

- During the **positive half cycle** of the sinusoidal input signal, the voltage present at the non-inverting terminal of op-amp is greater than zero volts. Hence, the output value of a non-inverting comparator will be equal to +Vsat+Vsat during the positive half cycle of the sinusoidal input signal.
- Similarly, during the **negative half cycle** of the sinusoidal input signal, the voltage present at the non-inverting terminal of op-amp is less than zero volts. Hence, the output value of non-inverting comparator will be equal to −Vsat−Vsat during the negative half cycle of the sinusoidal input signal.

The following figure shows the **input and output waveforms** of a non-inverting comparator, when the reference voltage is zero volts.



From the figure shown above, we can observe that the output transitions either from +Vsat+Vsat to −Vsat−Vsat or from −Vsat−Vsat to +Vsat+Vsat whenever the sinusoidal input signal crosses zero volts. That means, the output changes its value when the input is crossing zero volts. Hence, the above circuit is also called as **non-inverting zero crossing detector**.

Log And Anti Log Amplifiers

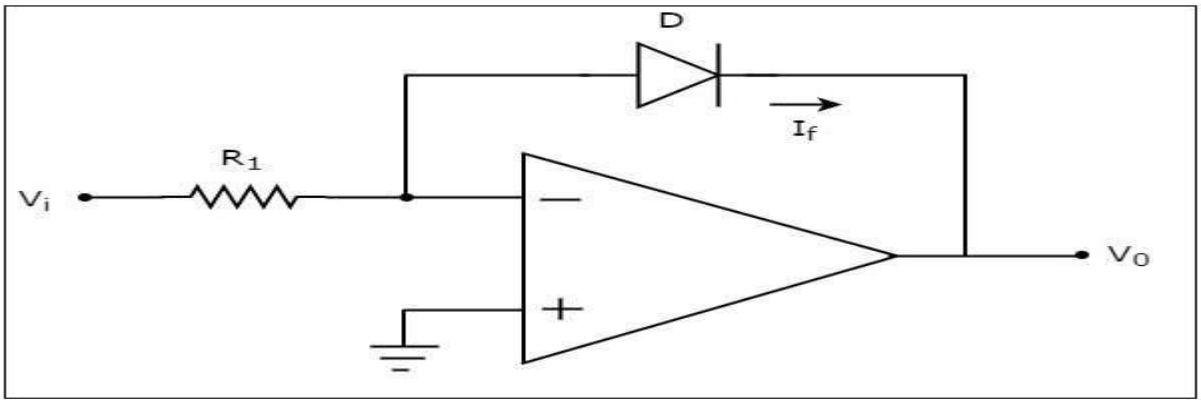
The electronic circuits which perform the mathematical operations such as logarithm and anti-logarithm (exponential) with an amplification are called as **Logarithmic amplifier** and **Anti-Logarithmic amplifier** respectively.

This chapter discusses about the **Logarithmic amplifier** and **Anti-Logarithmic amplifier** in detail. Please note that these amplifiers fall under non-linear applications.

Logarithmic Amplifier

A **logarithmic amplifier**, or a **log amplifier**, is an electronic circuit that produces an output that is proportional to the logarithm of the applied input. This section discusses about the op-amp based logarithmic amplifier in detail.

An op-amp based logarithmic amplifier produces a voltage at the output, which is proportional to the logarithm of the voltage applied to the resistor connected to its inverting terminal. The **circuit diagram** of an op-amp based logarithmic amplifier is shown in the following figure −



In the above circuit, the non-inverting input terminal of the op-amp is connected to ground. That means zero volts is applied at the non-inverting input terminal of the op-amp.

According to the **virtual short concept**, the voltage at the inverting input terminal of an op-amp will be equal to the voltage at its non-inverting input terminal. So, the voltage at the inverting input terminal will be zero volts.

The **nodal equation** at the inverting input terminal's node is −

$$0-ViR1+If=00-ViR1+If=0$$

$$=>If=ViR1.....Equation1=>If=ViR1.....Equation1$$

The following is the **equation for current** flowing through a diode, when it is in forward bias −

$$If=Ise(VfnVT).....Equation2If=Ise(VfnVT).....Equation2$$

where,

IsIs is the saturation current of the diode,
VfVf is the voltage drop across diode, when it is in forward bias,
VTVT is the diode's thermal equivalent voltage.

The **KVL equation** around the feedback loop of the op amp will be −

$$0-Vf-V0=00-Vf-V0=0$$

$$=>Vf=-V0=>Vf=-V0$$

Substituting the value of VfVf in Equation 2, we get −

$$If=Ise(-V0nVT).....Equation3If=Ise(-V0nVT).....Equation3$$

Observe that the left hand side terms of both equation 1 and equation 3 are same. Hence, equate the right hand side term of those two equations as shown below −

$$ViR1=Ise(-V0nVT)ViR1=Ise(-V0nVT)$$

$$ViR1Is=e(-V0nVT)ViR1Is=e(-V0nVT)$$

Applying **natural logarithm** on both sides, we get −

$$In(ViR1Is)=-V0nVTIn(ViR1Is)=-V0nVT$$

$$V0=-nVTIn(ViR1Is)V0=-nVTIn(ViR1Is)$$

Note that in the above equation, the parameters n, VTVT and IsIs are constants. So, the output voltage V0V0 will be proportional to the **natural logarithm** of the input voltage ViVi for a fixed value of resistance R1R1.

Therefore, the op-amp based logarithmic amplifier circuit discussed above will produce an output, which is proportional to the natural logarithm of the input voltage VTVT, when R1Is=1VR1Is=1V.

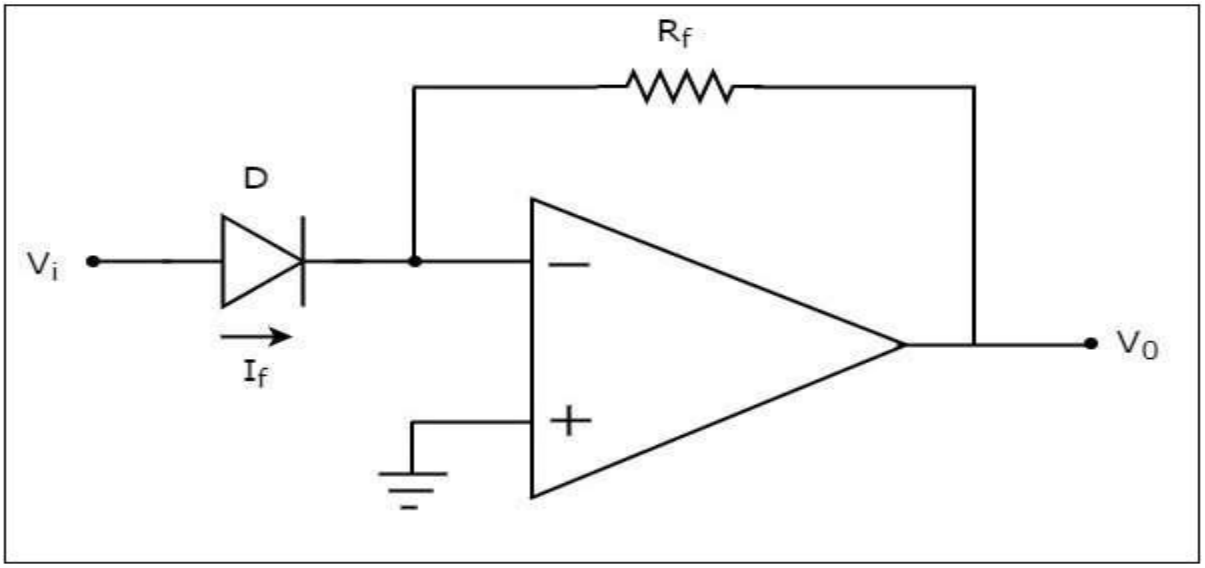
Observe that the output voltage V0V0 has a **negative sign**, which indicates that there exists a 180^0 phase difference between the input and the output.

Anti-Logarithmic Amplifier

An **anti-logarithmic amplifier**, or an **anti-log amplifier**, is an electronic circuit that produces an output that is proportional to the anti-logarithm of the applied input. This section discusses about the op-amp based anti-logarithmic amplifier in detail.

An op-amp based anti-logarithmic amplifier produces a voltage at the output, which is proportional to the anti-logarithm of the voltage that is applied to the diode connected to its inverting terminal.

The **circuit diagram** of an op-amp based anti-logarithmic amplifier is shown in the following figure −



In the circuit shown above, the non-inverting input terminal of the op-amp is connected to ground. It means zero volts is applied to its non-inverting input terminal.

According to the **virtual short concept**, the voltage at the inverting input terminal of op-amp will be equal to the voltage present at its non-inverting input terminal. So, the voltage at its inverting input terminal will be zero volts.

The **nodal equation** at the inverting input terminal's node is −

$$-If+0-V0Rf=0-If+0-V0Rf=0$$

$$=>-V0Rf=If=>-V0Rf=If$$

$$=>V0=-RfIf.....Equation4=>V0=-RfIf.....Equation4$$

We know that the equation for the current flowing through a diode, when it is in forward bias, is as given below −

$$If=Ise(VfnVT)If=Ise(VfnVT)$$

Substituting the value of IfIf in Equation 4, we get

$$V0=-Rf\{Ise(VfnVT)\}V0=-Rf\{Ise(VfnVT)\}$$

$$V0=-RfIse(VfnVT).....Equation5V0=-RfIse(VfnVT).....Equation5$$

The KVL equation at the input side of the inverting terminal of the op amp will be

$$Vi-Vf=0Vi-Vf=0$$

$$Vf=ViVf=Vi$$

Substituting, the value of □□ in the Equation 5, we get −

$$V0=-RfIse(VinVT)V0=-RfIse(VinVT)$$

Note that, in the above equation the parameters n, VTVT and IsIs are constants. So, the output voltage V0V0 will be proportional to the **anti-natural logarithm** (exponential) of the input voltage ViVi, for a fixed value of feedback resistance RfRf.

Therefore, the op-amp based anti-logarithmic amplifier circuit discussed above will produce an output, which is proportional to the anti-natural logarithm (exponential) of the input voltage ViVi when, RfIs=1VRfIs=1V. Observe that the output voltage V0V0 is having a **negative sign**, which indicates that there exists a 180^0 phase difference between the input and the output.

Rectifiers

AC and **DC** are two frequent terms that you encounter while studying the flow of electrical charge. **Alternating Current (AC)** has the property to change its state continuously. For example, if we consider a sine wave, the current flows in one direction for positive half cycle and in the opposite direction for negative half cycle. On the other hand, **Direct Current (DC)** flows only in one direction.

An electronic circuit, which produces either DC signal or a pulsated DC signal, when an AC signal is applied to it is called as a **rectifier**. This chapter discusses about op-amp based rectifiers in detail.

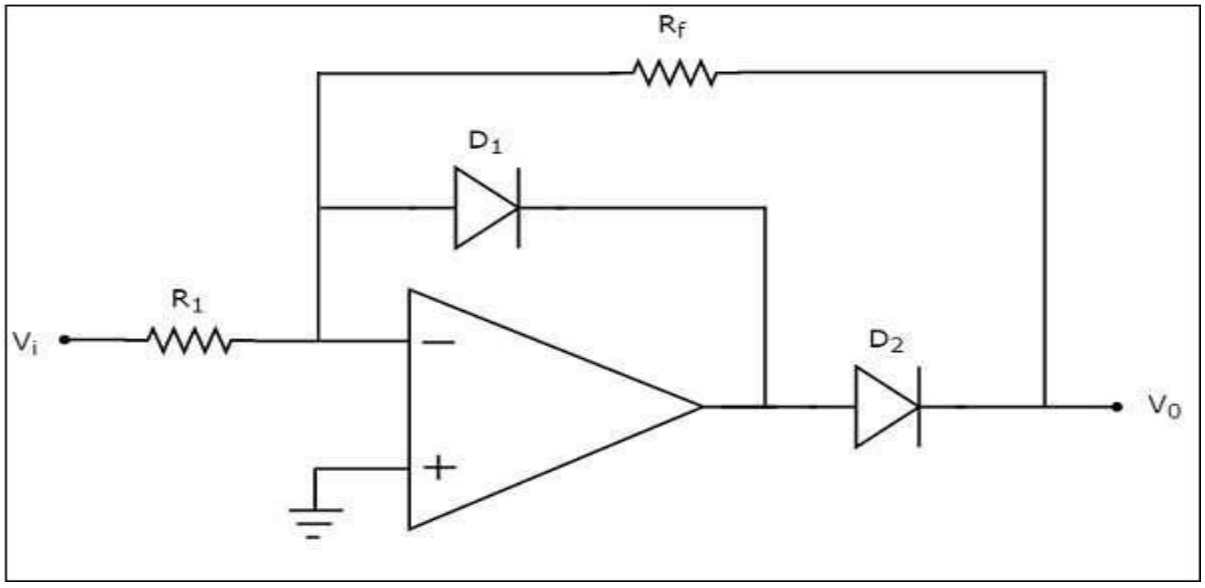
Types of Rectifiers

Rectifiers are classified into two types: **Half wave rectifier** and **Full wave rectifier**. This section discusses about these two types in detail.

Half wave Rectifier

A **half wave rectifier** is a rectifier that produces positive half cycles at the output for one half cycle of the input and zero output for the other half cycle of the input.

The **circuit diagram** of a half wave rectifier is shown in the following figure.



Observe that the circuit diagram of a half wave rectifier shown above looks like an inverting amplifier, with two diodes D_1 and D_2 in addition.

The **working** of the half wave rectifier circuit shown above is explained below

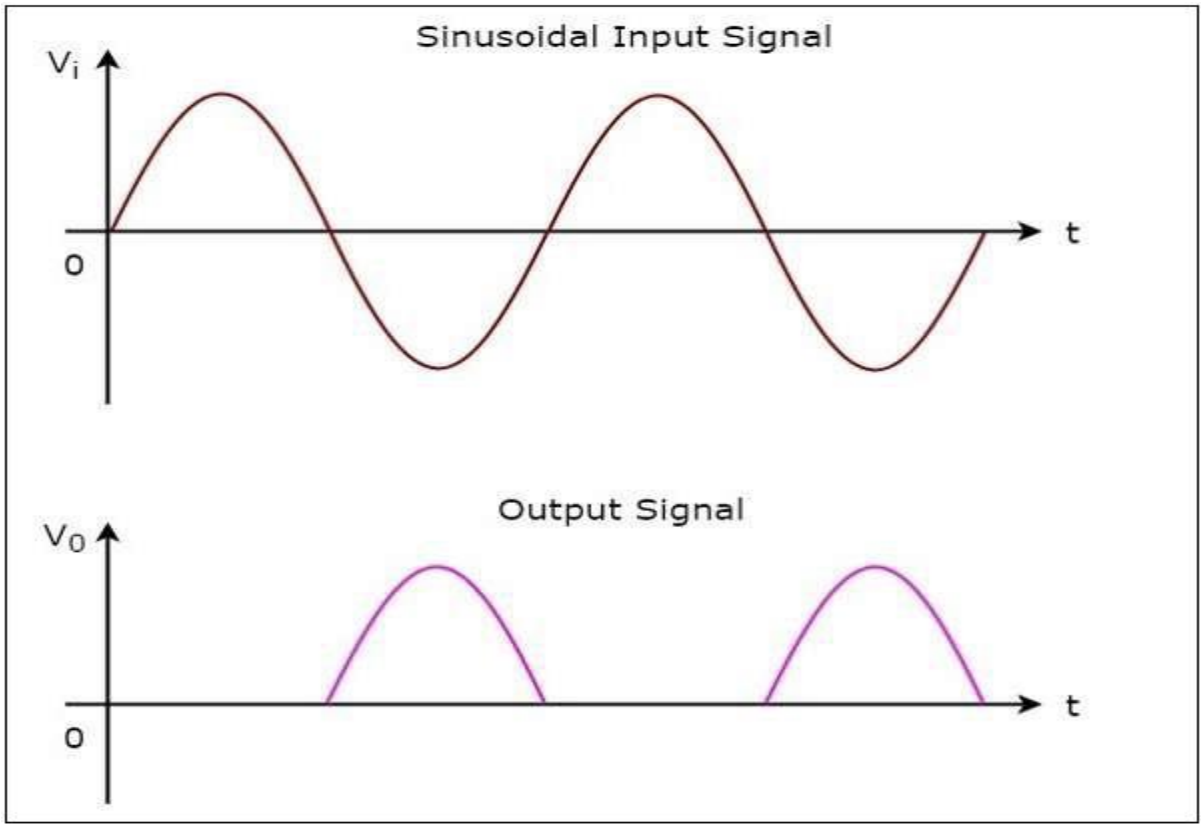
- For the **positive half cycle** of the sinusoidal input, the output of the op-amp will be negative. Hence, diode D_1 will be forward biased.
- When diode D_1 is in forward bias, output voltage of the op-amp will be -0.7 V. So, diode D_2 will be reverse biased. Hence, the **output voltage** of the above circuit is **zero** volts.
- Therefore, there is **no (zero) output** of half wave rectifier for the positive half cycle of a sinusoidal input.
- For the **negative half cycle** of sinusoidal input, the output of the op-amp will be positive. Hence, the diodes D_1 and D_2 will be reverse biased and forward biased respectively. So, the output voltage of above circuit will be −

$$V0=−(RfR1)V1V0=−(RfR1)V1$$

- Therefore, the output of a half wave rectifier will be a **positive half cycle** for a negative half cycle of the sinusoidal input.

Wave forms

The **input** and **output waveforms** of a half wave rectifier are shown in the following figure

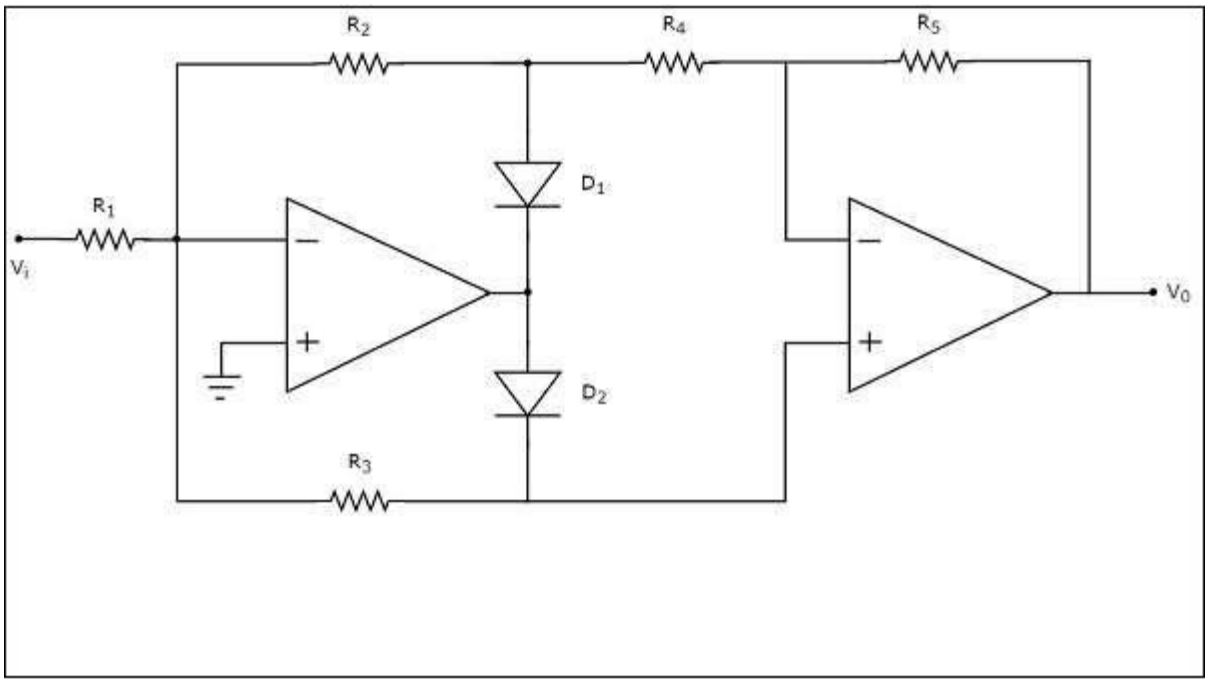


As you can see from the above graph, the half wave rectifier circuit diagram that we discussed will produce **positive half cycles** for negative half cycles of sinusoidal input and zero output for positive half cycles of sinusoidal input

Full wave Rectifier

A **full wave rectifier** produces positive half cycles at the output for both half cycles of the input.

The **circuit diagram** of a full wave rectifier is shown in the following figure −



The above circuit diagram consists of two op-amps, two diodes, D_1 & D_2 and five resistors, R_1 to R_5. The **working** of the full wave rectifier circuit shown above is explained below −

- For the **positive half cycle** of a sinusoidal input, the output of the first op-amp will be negative. Hence, diodes D_1 and D_2 will be forward biased and reverse biased respectively.
- Then, the output voltage of the first op-amp will be −

$$V01=−(R2R1)ViV01=−(R2R1)Vi$$

- Observe that the output of the first op-amp is connected to a resistor R_4, which is connected to the inverting terminal of the second op-amp. The voltage present at the non-inverting terminal of second op-amp is 0 V. So, the second op-amp with resistors, R_4 and R_4 acts as an **inverting amplifier**.
- The output voltage of the second op-amp will be

$$V0=−(R5R4)V01V0=−(R5R4)V01$$

Substituting the value of V01V01 in the above equation, we get −

$$=>V0=−(R5R4){−(R2R1)Vi}=>V0=−(R5R4){−(R2R1)Vi}$$

$$=>V0=(R2R5R1R4)Vi=>V0=(R2R5R1R4)Vi$$

- Therefore, the output of a full wave rectifier will be a positive half cycle for the **positive half cycle** of a sinusoidal input. In this case, the gain of the output is R2R5R1R4R2R5R1R4. If we consider R1=R2=R4=R5=RR1=R2=R4=R5=R, then the gain of the output will be one.
- For the **negative half cycle** of a sinusoidal input, the output of the first op-amp will be positive. Hence, diodes D_1 and D_2 will be reverse biased and forward biased respectively.
- The output voltage of the first op-amp will be −

$$V01=−(R3R1)ViV01=−(R3R1)Vi$$

- The output of the first op-amp is directly connected to the non-inverting terminal of the second op-amp. Now, the second op-amp with resistors, R_4 and R_5 acts as a **non-inverting amplifier**.

  The output voltage of the second op-amp will be −

$$V0=(1+R5R4)V01V0=(1+R5R4)V01$$

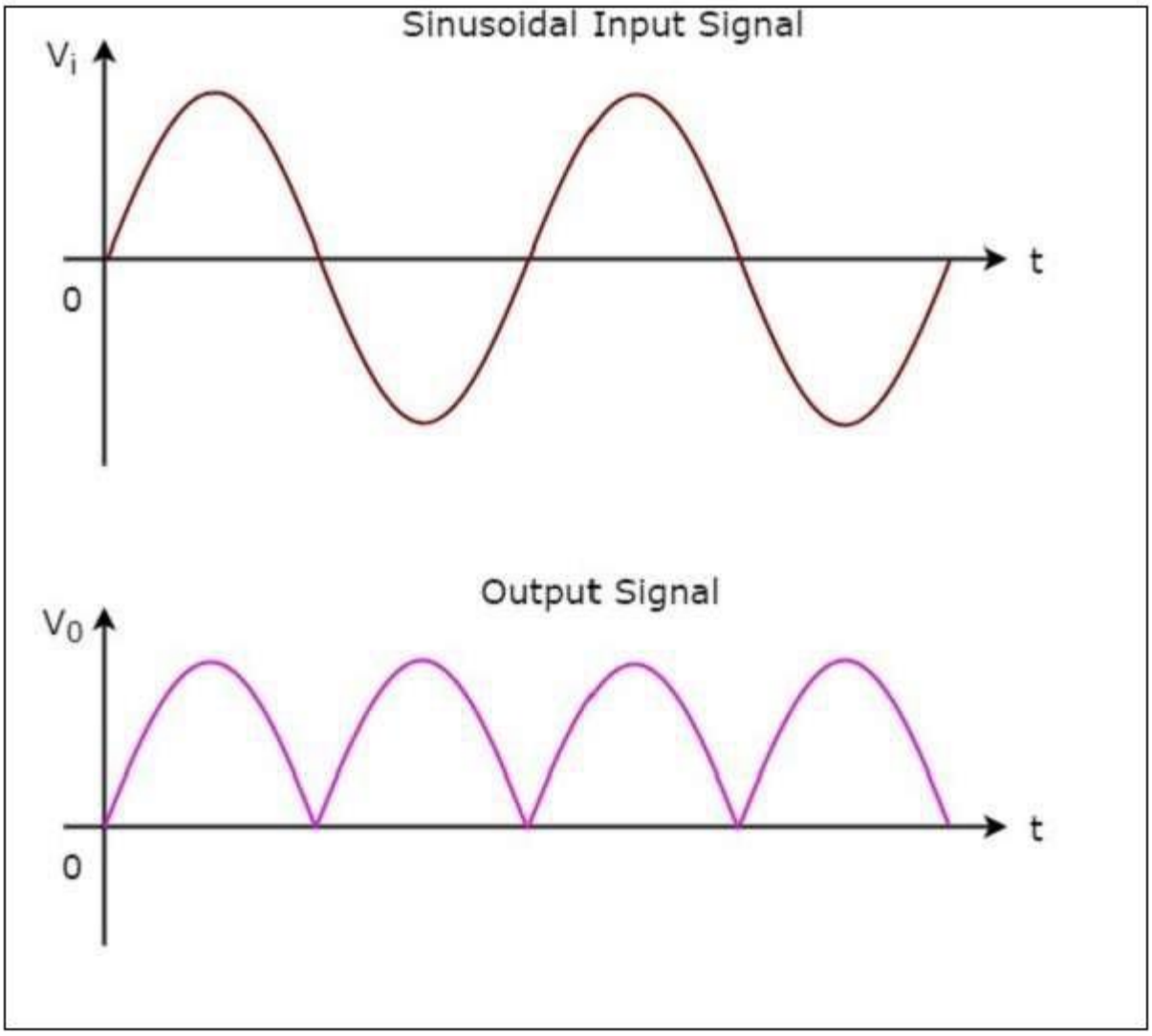
  Substituting the value of V01V01 in the above equation, we get

$$=>V0=(1+R5R4){−(R3R1)Vi}=>V0=(1+R5R4){−(R3R1)Vi}$$

$$=>V0=−(R3R1)(1+R5R4)Vi=>V0=−(R3R1)(1+R5R4)Vi$$

- Therefore, the output of a full wave rectifier will be a **positive half cycle** for the negative half cycle of sinusoidal input also. In this case, the magnitude of the gain of the output is (R3R1)(1+R5R4)(R3R1)(1+R5R4).
- If we consider R1=2R3=R4=R5=RR1=2R3=R4=R5=R then the gain of the output will be **one**.

The **input** and **output waveforms** of a full wave rectifier are shown in the following figure

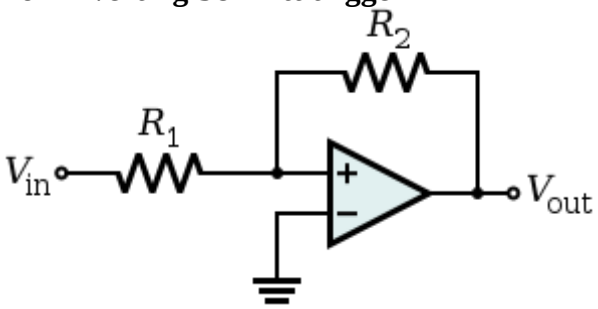


As you can see in the above figure, the full wave rectifier circuit diagram that we considered will produce only **positive half cycles** for both positive and negative half cycles of a sinusoidal input.

SCHMITT TRIGGER

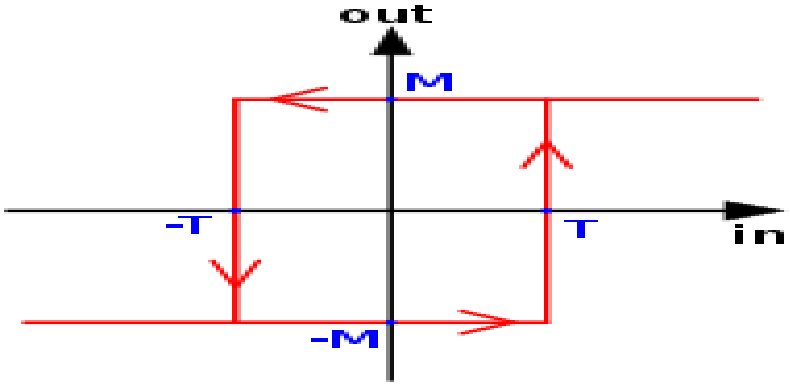
Schmitt triggers are commonly implemented using an operational amplifier or a dedicated comparator. An open-loop op-amp and comparator may be considered as an analog-digital device having analog inputs and a digital output that extracts the sign of the voltage difference between its two inputs. The positive feedback is applied by adding a part of the output voltage to the input voltage in series or parallel manner. Due to the extremely high op-amp gain, the loop gain is also high enough and provides the avalanche-like process.

Non-inverting Schmitt trigger



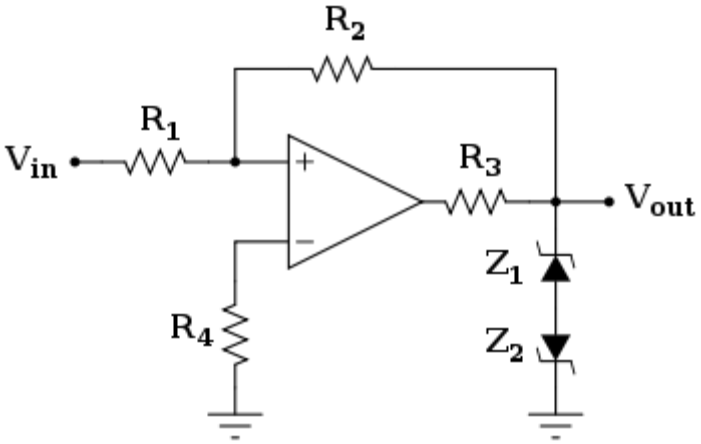
Schmitt trigger implemented by a non-inverting comparator. In this circuit, the two resistors R_1 and R_2 form a parallel voltage summer. It adds a part of the output voltage to the input voltage thus augmenting it during and after switching that occurs when the resulting voltage is near ground. This *parallel positive feedback* creates the needed hysteresis that is controlled by the proportion between the resistances of R_1 and R_2. The output of the parallel voltage summer is single-ended (it produces voltage with respect to ground) so the circuit does not need an amplifier with a differential input. Since conventional op-amps have a differential input, the inverting input is grounded to make the reference point zero volts.

The output voltage always has the same sign as the *op-amp input voltage* but it does not always have the same sign as the *circuit input voltage* (the signs of the two input voltages can differ). When the circuit input voltage is above the high threshold or below the low threshold, the output voltage has the same sign as the *circuit input voltage* (the circuit is non-inverting). It acts like a comparator that switches at a different point depending on whether the output of the comparator is high or low. When the circuit input voltage is between the thresholds, the output voltage is undefined and it depends on the last state (the circuit behaves as an elementary latch).



Typical transfer function of a non-inverting Schmitt trigger like the circuit above.
For instance, if the Schmitt trigger is currently in the high state, the output will be at the positive power supply rail ($+V_S$). The output voltage V_+ of the resistive summer can be found by applying the superposition theorem:

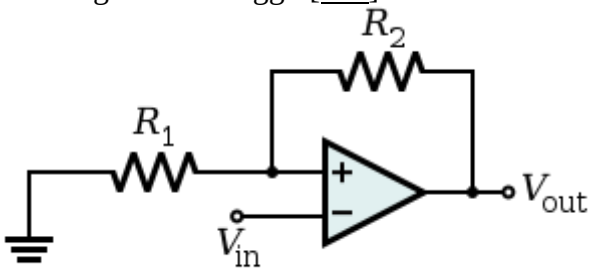
The comparator will switch when $V_+=0$. Then (the same result can be obtained by applying the current conservation principle). So must drop below to get the output to switch. Once the comparator output has switched to $-V_S$, the threshold becomes to switch back to high. So this circuit creates a switching band centered on zero, with trigger levels (it can be shifted to the left or the right by applying a bias voltage to the inverting input). The input voltage must rise above the top of the band, and then below the bottom of the band, for the output to switch on (plus) and then back off (minus). If R_1 is zero or R_2 is infinity (i.e., an open circuit), the band collapses to zero width, and it behaves as a standard comparator. The transfer characteristic is shown in the picture on the left. The value of the threshold T is given by and the maximum value of the output M is the power supply rail.



A practical Schmitt trigger configuration with precise thresholds
A unique property of circuits with parallel positive feedback is the impact on the input source.[*citation needed*] In circuits with negative parallel feedback (e.g., an inverting amplifier), the virtual ground at the inverting input separates the input source from the op-amp output. Here there is no virtual ground, and the steady op-amp output voltage is applied through R_1-R_2 network to the input source. The op-amp output passes an opposite current through the input source (it injects current into the source when the input voltage is positive and it draws current from the source when it is negative).

A practical Schmitt trigger with precise thresholds is shown in the figure on the right. The transfer characteristic has exactly the same shape of the previous basic configuration, and the threshold values are the same as well. On the other hand, in the previous case, the output voltage was depending on the power supply, while now it is defined by the Zener diodes (which could also be replaced with a single double-anode Zener diode). In this configuration, the output levels can be modified by appropriate choice of Zener diode, and these levels are resistant to power supply fluctuations (i.e., they increase the PSRR of the comparator). The resistor R_3 is there to limit the current through the diodes, and the resistor R_4 minimizes the input voltage offset caused by the comparator's input leakage currents (see *limitations of real op-amps*).

Inverting Schmitt trigger[edit]



Schmitt trigger implemented by an inverting comparator

In the inverting version, the attenuation and summation are separated. The two resistors R_1 and R_2 act only as a "pure" attenuator (voltage divider). The input loop acts as a simple series voltage summer that adds a part of the output voltage in series to the circuit input voltage. This *series positive feedback* creates the needed hysteresis that is controlled by the proportion between the resistances of R_1 and the whole resistance (R_1 and R_2). The effective voltage applied to the op-amp input is floating so the op-amp must have a differential input.

The circuit is named *inverting* since the output voltage always has an opposite sign to the input voltage when it is out of the hysteresis cycle (when the input voltage is above the high threshold or below the low threshold). However, if the input voltage is within the hysteresis cycle (between the high and low thresholds), the circuit can be inverting as well as non-inverting. The output voltage is undefined and it depends on the last state so the circuit behaves like an elementary latch.

To compare the two versions, the circuit operation will be considered at the same conditions as above. If the Schmitt trigger is currently in the high state, the output will be at the positive power supply rail ($+V_S$). The output voltage V_+ of the voltage divider is:

The comparator will switch when $V_{in} = V_+$. So must exceed above this voltage to get the output to switch. Once the comparator output has switched to $-V_S$, the threshold becomes to switch back to high. So this circuit creates a switching band centered on zero, with trigger levels (it can be shifted to the left or the right by connecting R_1 to a bias voltage). The input voltage must rise above the top of the band, and then below the bottom of the band, for the output to switch off (minus) and then back on (plus). If R_1 is zero (i.e., a short circuit) or R_2 is infinity, the band collapses to zero width, and it behaves as a standard comparator.

In contrast with the parallel version, this circuit does not impact on the input source since the source is separated from the voltage divider output by the high op-amp input differential impedance.

In the inverting amplifier voltage drop across resistor (R1) decides the reference voltages i.e.,upper threshold voltage (V+) and lower threshold voltages (V-) for the comparison with input signal applied. These voltages are fixed as the output voltage and resistor values are fixed.

so by changing the drop across (R1) threshold voltages can be varied. By adding a bias voltage in series with resistor (R1) drop across it can be varied, which can change threshold voltages. Desired values of reference voltages can be obtained by varying bias voltage.

The above equations can be modified as

Applications

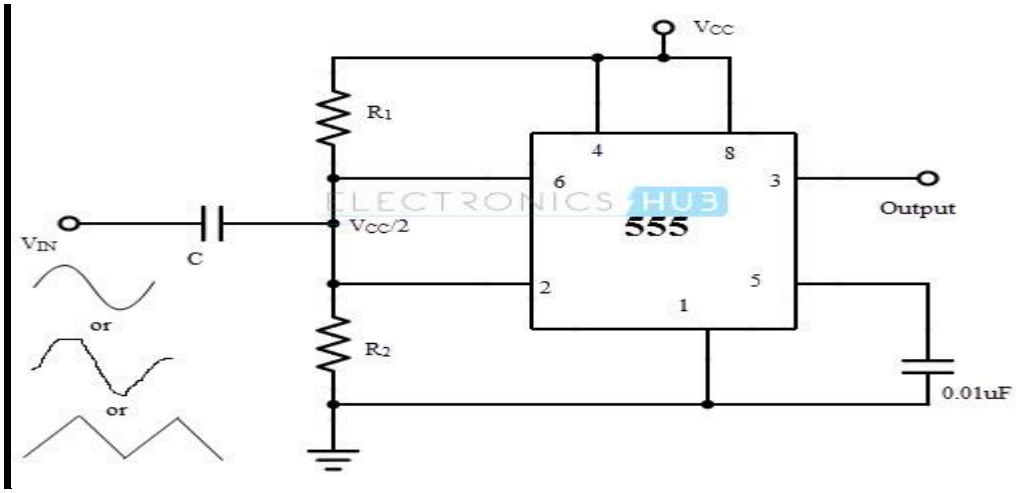
Schmitt triggers are typically used in open loop configurations for noise immunity and closed loop configurations to implement function generators.

- Analog to digital conversion*:* The Schmitt trigger is effectively a one bit analog to digital converter. When the signal reaches a given level it switches from its low to high state.
- Level detection*:* The Schmitt trigger circuit is able to provide level detection. When undertaking this application, it is necessary that the hysteresis voltage is taken into account so that the circuit switches on the required voltage.
- Line reception*:* When running a data line that may have picked up noise into a logic gate it is necessary to ensure that a logic output level is only changed as the data changed and not as a result of spurious noise that may have been picked up. Using a Schmitt trigger broadly enables the peak to peak noise to reach the level of the hysteresis before spurious triggering may occur.

Schmitt Trigger

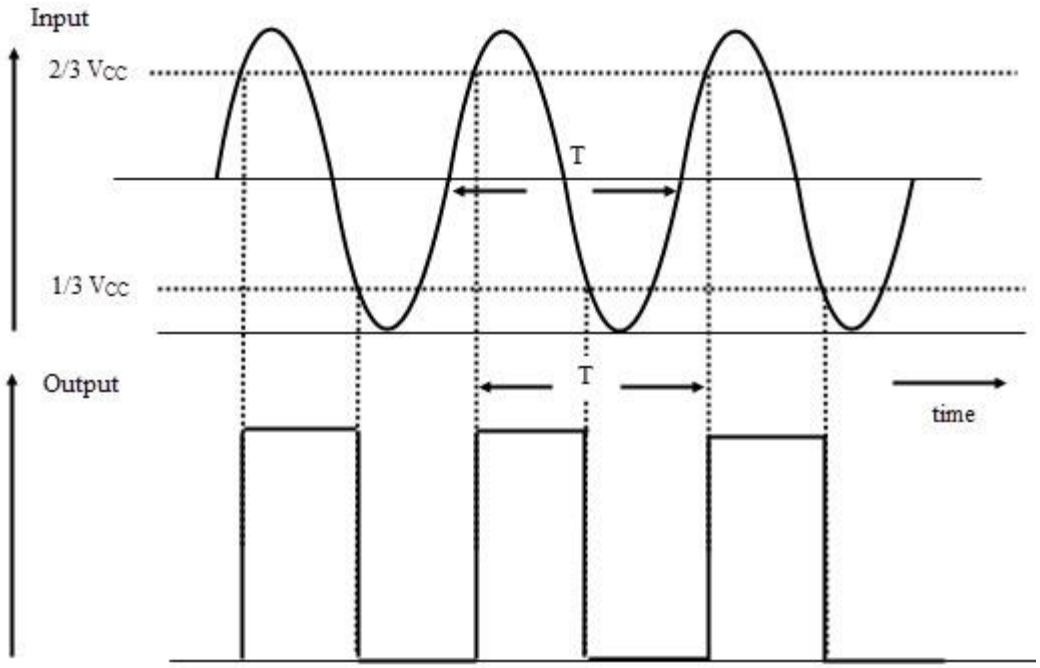
- The high and low transitions on the inputs of most of the CMOS devices should be fast edges. If the edges are not fast enough, they tend to provide more current and this might damage the device. Analog signals are generally not perfect and might not have clean edges all the times. Schmitt Trigger is a special type of comparator that is used to avoid such signals.
- A comparator is a device that compares two voltages and the outcome is the indication of whether one voltage is higher than the other or not. Schmitt trigger, also called as Regenerative Comparator, compares the input voltage to two reference voltages and produces an equivalent output. The output of a Schmitt trigger is always a square or rectangular wave irrespective of the shape of the input. It is often used when we need to do the following:
- Convert sine wave to square wave
- To clean up the noisy signals
- To convert slow edges (like in a triangular wave) into fast edges (like a square wave)
- Schmitt can be constructed from a 555 timer. Some of the other function of the 555 timer, apart from the timer operation, is to use the two internal comparators as independent units to form a Schmitt Trigger. The general operation of the Schmitt trigger built from a 555 timer is inverting but the discussion will be for non-inverting.

Circuit of 555 timer as Schmitt Trigger

- The following circuit shows the structure of a 555 timer used as a Schmitt trigger.
- 

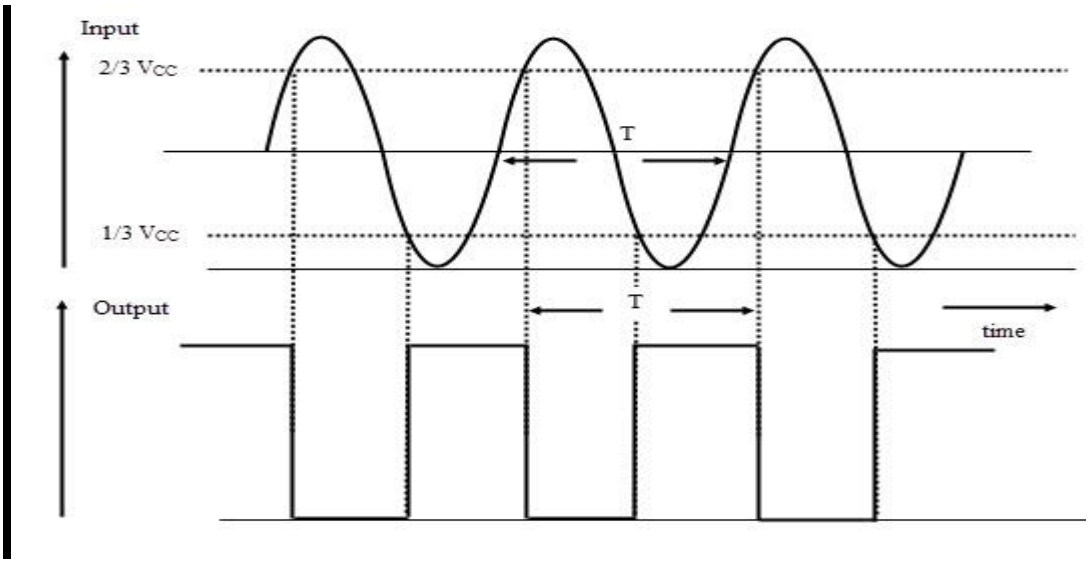
- Pins 4 and 8 are connected to the supply (VCC). The pins 2 and 6 are tied together and the input is given to this common point through a capacitor C. this common point is supplied with an external bias voltage of VCC / 2 with the help of the voltage divider circuit formed by the resistors R1 and R2.
- The important characteristic of the Schmitt trigger is Hysteresis. The output of the Schmitt trigger is high if the input voltage is greater than the upper threshold value and the output of the Schmitt trigger is low if the input voltage is lower than the lower threshold value.
- The output retains its value when the input is between the two threshold values. The usage of two threshold values is called Hysteresis and the Schmitt trigger acts as a memory element (a bistable multivibrator or a flip-flop).
- The threshold values in this case are 2/3 VCC and 1/3 VCC i.e. the upper comparator trips at 2/3 VCC and the lower comparator trips at 1/3 VCC. The input voltage is compared to these threshold values by the individual comparators and the flip-flop is SET or RESET accordingly. Based on this the output becomes high or low.

- When a sine wave of amplitude greater than VCC / 6 is applied at the input, the flip-flop is set and reset alternately for the positive cycle and the negative cycle. The output is a square wave and the waveforms for input sine wave and output square wave are shown below.



Inverting Schmitt Trigger

- The normal operation of the 555 timer as a Schmitt trigger is inverting in nature. When the trigger input, which is same as the external input, falls below the threshold value of 1/3 VCC, the output of the lower comparator goes high and the flip-flop is SET and the output at pin 3 goes high.
- Similarly, when the threshold input, which is same as the external input, rises above the threshold value of 2/3 VCC, the output of the upper comparator goes high and the flip-flop is RESET and the output at pin 3 goes low.
- The waveform of the inverting Schmitt trigger is shown below.



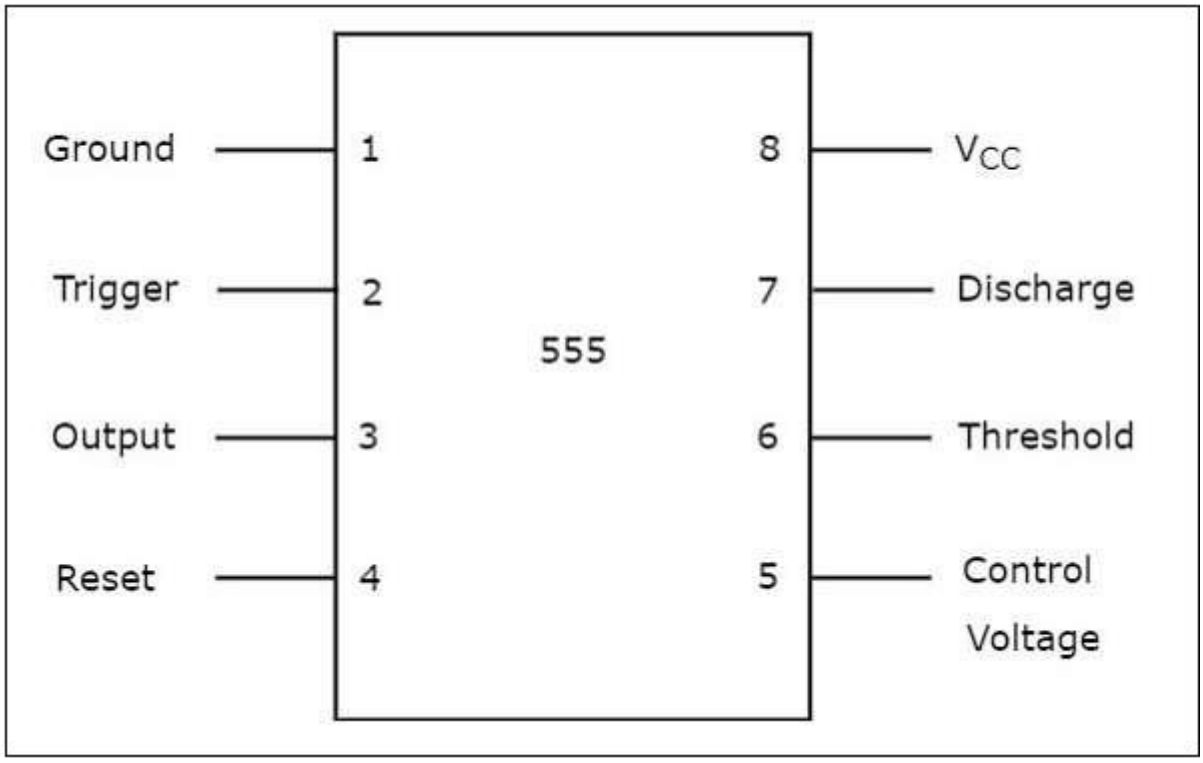
MODULE-III - 555 Timers

The **555 Timer** IC got its name from the three 5KΩ resistors that are used in its voltage divider network. This IC is useful for generating accurate time delays and oscillations.

Pin Diagram and Functional Diagram:

Pin Diagram:

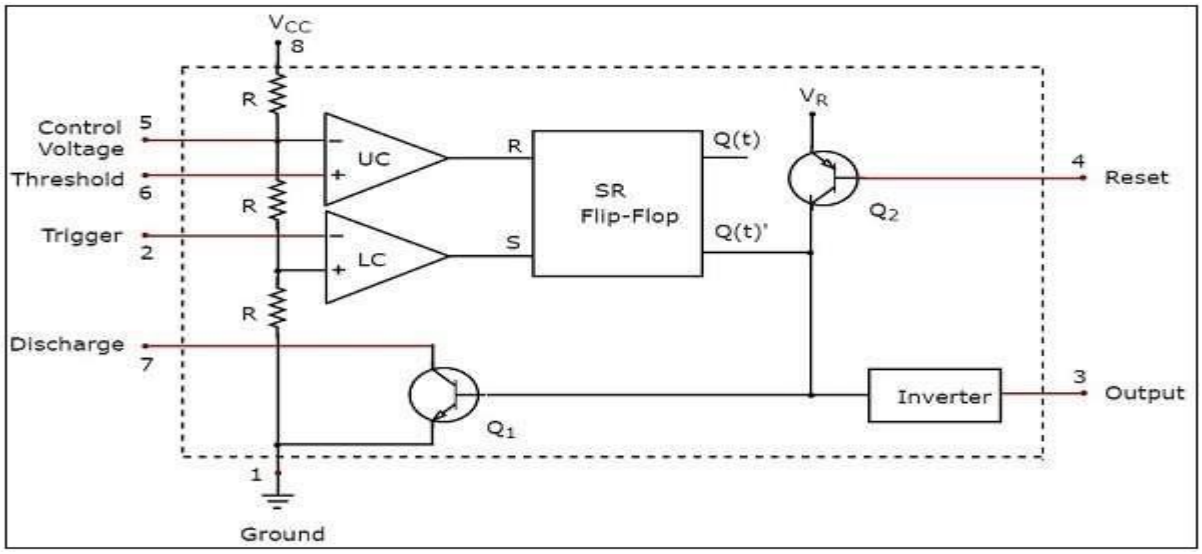
The 555 Timer IC is an 8 pin mini Dual-Inline Package (DIP). The **pin diagram** of a 555 Timer:



The significance of each pin is self-explanatory from the above diagram. This 555 Timer IC can be operated with a DC supply of +5V to +18V. It is mainly useful for generating **non-sinusoidal** wave forms like square, ramp, pulse & etc

Functional Diagram:

The pictorial representation showing the internal details of a 555 Timer is known as functional diagram. The **functional diagram** of 555 Timer IC is shown below:



Observe that the functional diagram of 555 Timer contains a voltage divider network, two comparators, one SR flip-flop, two transistors and an inverter. This section discusses about the purpose of each block or component in detail −

Voltage Divider Network

- The voltage divider network consists of a three 5KΩ5KΩ resistors that are connected in series between the supply voltage VccVcc and ground.
- This network provides a voltage of Vcc3Vcc3 between a point and ground, if there exists only one 5KΩ5KΩ resistor. Similarly, it provides a voltage of 2Vcc32Vcc3 between a point and ground, if there exists only two 5KΩ5KΩ resistors.

Comparator

- The functional diagram of a 555 Timer IC consists of two comparators: an Upper Comparator (UC) and a Lower Comparator (LC).
- Recall that a **comparator** compares the two inputs that are applied to it and produces an output.
- If the voltage present at the non-inverting terminal of an op-amp is greater than the voltage present at its inverting terminal, then the output of comparator will be +Vsat+Vsat. This can be considered as **Logic High** ('1') in digital representation.
- If the voltage present at the non-inverting terminal of op-amp is less than or equal to the voltage at its inverting terminal, then the output of comparator will be −Vsat−Vsat. This can be considered as **Logic Low** ('0') in digital representation.

SR Flip-Flop

- Recall that a **SR flip-flop** operates with either positive clock transitions or negative clock transitions. It has two inputs: S and R, and two outputs: Q(t) and Q(t)'. The outputs, Q(t) & Q(t)' are complement to each other.
- The following table shows the **state table** of a SR flip-flop:

S	R	Q(t+1)

0	0	Q(t)
0	1	0
1	0	1
1	1	-

- Here, Q(t) & Q(t+1) are present state & next state respectively. So, SR flip-flop can be used for one of these three functions such as Hold, Reset & Set based on the input conditions, when positive (negative) transition of clock signal is applied.
- The outputs of Lower Comparator (LC) and Upper Comparator (UC) are applied as **inputs of SR flip-flop** as shown in the functional diagram of 555 Timer IC.

Transistors and Inverter

- The functional diagram of a 555 Timer IC consists of one npn transistor Q1Q1 and one pnp transistor Q2Q2. The npn transistor Q1Q1 will be turned ON if its base to emitter voltage is positive and greater than cut-in voltage. Otherwise, it will be turned-OFF.
- The pnp transistor Q2Q2 is used as **buffer** in order to isolate the reset input from SR flip-flop and npn transistor Q1Q1.
- The **inverter** used in the functional diagram of a 555 Timer IC not only performs the inverting action but also amplifies the power level.

The 555 Timer IC can be used in mono stable operation in order to produce a pulse at the output. Similarly, it can be used in astable operation in order to produce a square wave at the output.

Phase Locked Loops

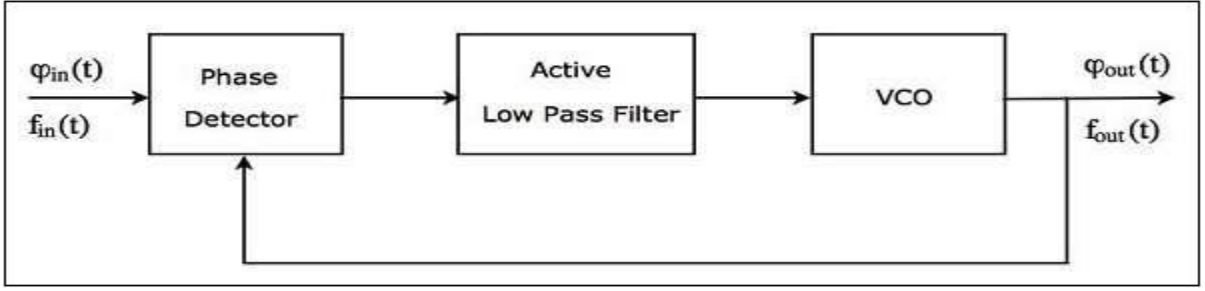
Phase Locked Loop **(PLL)** is one of the vital blocks in linear systems. It is useful in communication systems such as radars, satellites, FMs, etc.

Block Diagram of PLL:

A Phase Locked Loop (PLL) mainly consists of the following **three blocks** −

- Phase Detector
- Active Low Pass Filter
- Voltage Controlled Oscillator (VCO)

The **block diagram** of PLL is shown in the following figure −



The output of a phase detector is applied as an input of active low pass filter. Similarly, the output of active low pass filter is applied as an input of VCO.

The **working** of a PLL is as follows −

- **Phase detector** produces a DC voltage, which is proportional to the phase difference between the input signal having frequency of finfin and feedback (output) signal having frequency of fout.
- A **Phase detector** is a multiplier and it produces two frequency components at its output − sum of the frequencies finfin and foutfout and difference of frequencies finfin & foutfout.
- An **active low pass filter** produces a DC voltage at its output, after eliminating high frequency component present in the output of the phase detector. It also amplifies the signal.
- A **VCO** produces a signal having a certain frequency, when there is no input applied to it. This frequency can be shifted to either side by applying a DC voltage to it. Therefore, the frequency deviation is directly proportional to the DC voltage present at the output of a low pass filter.

The above operations take place until the VCO frequency equals to the input signal frequency. Based on the type of application, we can use either the output of active low pass filter or output of a VCO. PLLs are used in many **applications** such as FM demodulator, clock generator etc.

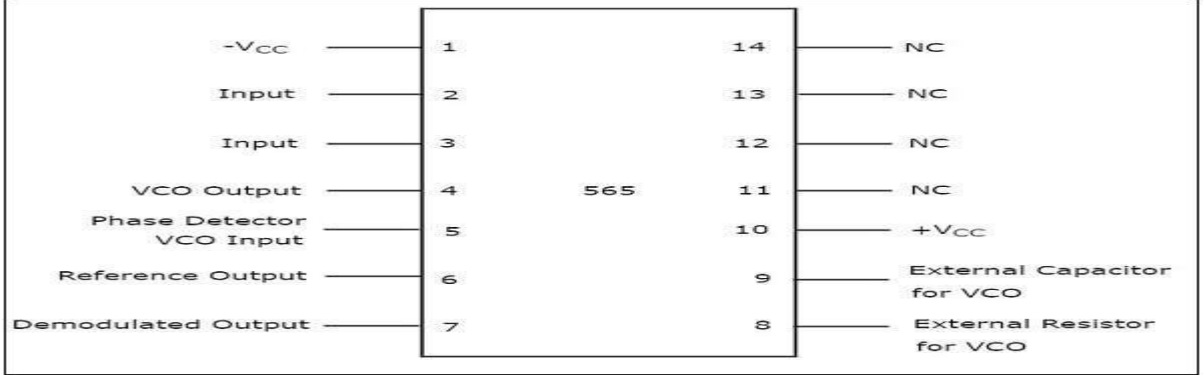
PLL operates in one of the **following three modes** −

- Free running mode
- Capture mode
- Lock mode

Initially, PLL operates in **free running mode** when no input is applied to it. When an input signal having some frequency is applied to PLL, then the output signal frequency of VCO will start change. At this stage, the PLL is said to be operating in the **capture mode**. The output signal frequency of VCO will change continuously until it is equal to the input signal frequency. Now, it is said to be PLL is operating in the **lock mode**.

IC 565:

IC 565 is the most commonly used in phase locked loop IC. It is a 14 pin Dual-Inline Package (DIP). The **pin diagram** of IC 565 is shown in the following figure −



The purpose of each pin is self-explanatory from the above diagram. Out of 14 pins, only 10 pins (pin number 1 to 10) are utilized for the operation of PLL. So, the remaining 4 pins (pin number 11 to 14) are labelled with NC (No Connection).

The **VCO** produces an output at pin number 4 of IC 565, when the pin numbers 2 and 3 are grounded. Mathematically, we can write the output frequency, fout of the VCO:

$$fout=0.25R_VC_V$$

where, R_V is the external resistor that is connected to the pin number 8

C_V is the external capacitor that is connected to the pin number 9

- By choosing proper values of R_V and C_V, we can determine the output frequency, fout of VCO.
- **Pin numbers 4 and 5** are to be shorted with an external wire so that the output of VCO can be applied as one of the inputs of phase detector.
- IC 565 has an internal resistance of 3.6KΩ. A capacitor, C has to be connected between pin numbers 7 and 10 in order to make a **low pass filter** with that internal resistance.

Module-IV:Voltage Regulators

The function of a voltage regulator is to maintain a constant DC voltage at the output irrespective of voltage fluctuations at the input and (or) variations in the load current. In other words, voltage regulator produces a regulated DC output voltage.

Voltage regulators are also available in Integrated Circuits (IC) forms. These are called as voltage regulator ICs.

Types of Voltage Regulators

There are two types of voltage regulators −

- Fixed voltage regulator
- Adjustable voltage regulator

Fixed voltage regulator:

A fixed voltage regulator produces a fixed DC output voltage, which is either positive or negative. In other words, some fixed voltage regulators produce positive fixed DC voltage values, while others produce negative fixed DC voltage values.

78xx voltage regulator ICs produce positive fixed DC voltage values, whereas, 79xx voltage regulator ICs produce negative fixed DC voltage values.

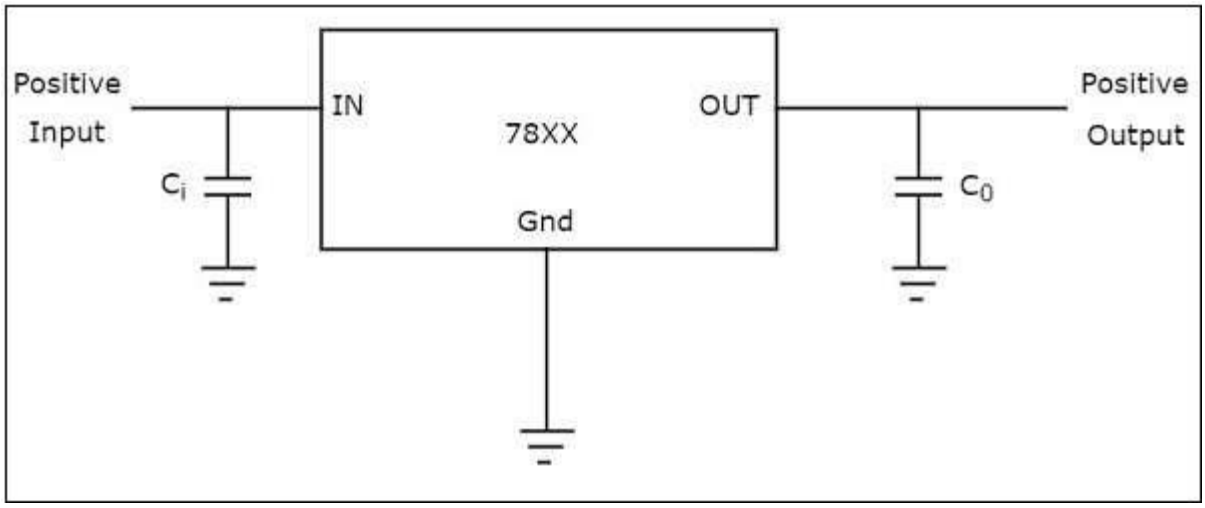
The following points are to be noted while working with 78xx and 79xx voltage regulator ICs −

- "xx" corresponds to a two-digit number and represents the amount (magnitude) of voltage that voltage regulator IC produces.
- Both 78xx and 79xx voltage regulator ICs have 3 pins each and the third pin is used for collecting the output from them.
- The purpose of the first and second pins of these two types of ICs is different −
    - The first and second pins of 78xx voltage regulator ICs are used for connecting the input and ground respectively.
    - The first and second pins of 79xx voltage regulator ICs are used for connecting the ground and input respectively.

Examples:

- 7805 voltage regulator IC produces a DC voltage of +5 volts.
- 7905 voltage regulator IC produces a DC voltage of -5 volts.

The following figure shows how to produce a fixed positive voltage at the output by using a fixed positive voltage regulator with necessary connections.



In the above figure that shows a fixed positive voltage regulator, the input capacitor C_i is used to prevent unwanted oscillations and the output capacitor, C_0 acts as a line filter to improve transient response.

Adjustable voltage regulator

An adjustable voltage regulator produces a DC output voltage, which can be adjusted to any other value of certain voltage range. Hence, adjustable voltage regulator is also called as a variable voltage regulator.

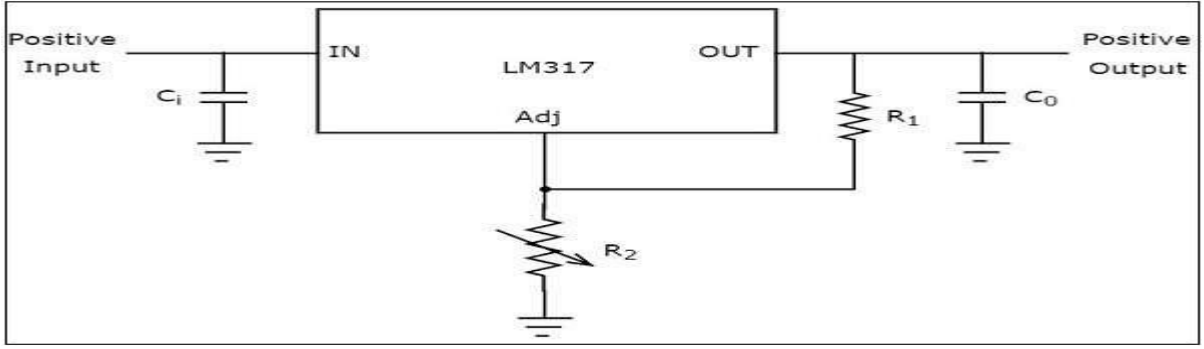
The DC output voltage value of an adjustable voltage regulator can be either positive or negative.

LM317 voltage regulator IC

LM317 voltage regulator IC can be used for producing a desired positive fixed DC voltage value of the available voltage range.

LM317 voltage regulator IC has 3 pins. The first pin is used for adjusting the output voltage, second pin is used for collecting the output and third pin is used for connecting the input.

The adjustable pin (terminal) is provided with a variable resistor which lets the output to vary between a wide range.



The above figure shows an unregulated power supply driving a LM 317 voltage regulator IC, which is commonly used. This IC can supply a load current of 1.5A over an adjustable output range of 1.25 V to 37 V.

Data Converters

All the real world quantities are analog in nature. We can represent these quantities electrically as analog signals. An analog signal is a time varying signal that has any number of values (variations) for a given time slot.

In contrast to this, a digital signal varies suddenly from one level to another level and will have only finite number of values (variations) for a given time slot.

This chapter discusses about the types of data converters and their specifications.

Types of Data Converters:

The electronic circuits, which can be operated with analog signals are called as analog circuits. Similarly, the electronic circuits, which can be operated with digital signals are called as digital circuits. A data converter is an electronic circuit that converts data of one form to another.

There are two types of data converters −

- Analog to Digital Converter
- Digital to Analog Converter

If we want to connect the output of an analog circuit as an input of a digital circuit, then we have to place an interfacing circuit between them. This interfacing circuit that converts the analog signal into digital signal is called as Analog to Digital Converter.

Similarly, if we want to connect the output of a digital circuit as an input of an analog circuit, then we have to place an interfacing circuit between them. This interfacing circuit that converts the digital signal into an analog signal is called as Digital to Analog Converter.

Specifications:

The following are the specifications that are related to data conversions −

- Resolution
- Conversion Time

Resolution:

Resolution is the minimum amount of change needed in an analog input voltage for it to be represented in binary (digital) output. It depends on the number of bits that are used in the digital output.

Mathematically, resolution can be represented as

$$\text{Resolution}=\frac{1}{2^N}$$

where, ‘N’ is the number of bits that are present in the digital output.

From the above formula, we can observe that there exists an inverse relationship between the resolution and number of bits. Therefore, resolution decreases as the number of bits increases and vice-versa.

Resolution can also be defined as the ratio of maximum analog input voltage that can be represented in binary and the equivalent binary number.

Mathematically, resolution can be represented as

$$\text{Resolution}=\frac{V_{FS}}{2^N}$$

where, V_{FS} is the full scale input voltage or maximum analog input voltage,

‘N’ is the number of bits that are present in the digital output.

Conversion Time:

The amount of time required for a data converter in order to convert the data (information) of one form into its equivalent data in other form is called as conversion time. Since we have two types of data converters, there are two types of conversion times as follows

- Analog to Digital Conversion time
- Digital to Analog Conversion time

The amount of time required for an Analog to Digital Converter (ADC) to convert the analog input voltage into its equivalent binary (digital) output is called as Analog to Digital conversion time. It depends on the number of bits that are used in the digital output.

The amount of time required for a Digital to Analog Converter (DAC) to convert the binary (digital) input into its equivalent analog output voltage is called as Digital to Analog conversion time. It depends on the number of bits that are present in the binary (digital) input.

Digital to Analog Converters

A Digital to Analog Converter (DAC) converts a digital input signal into an analog output signal. The digital signal is represented with a binary code, which is a combination of bits 0 and 1. This chapter deals with Digital to Analog Converters in detail.

The block diagram of DAC is shown in the following figure −

A Digital to Analog Converter (DAC) consists of a number of binary inputs and a single output. In general, the number of binary inputs of a DAC will be a power of two.

Types of DACs:

There are **two types** of DACs:

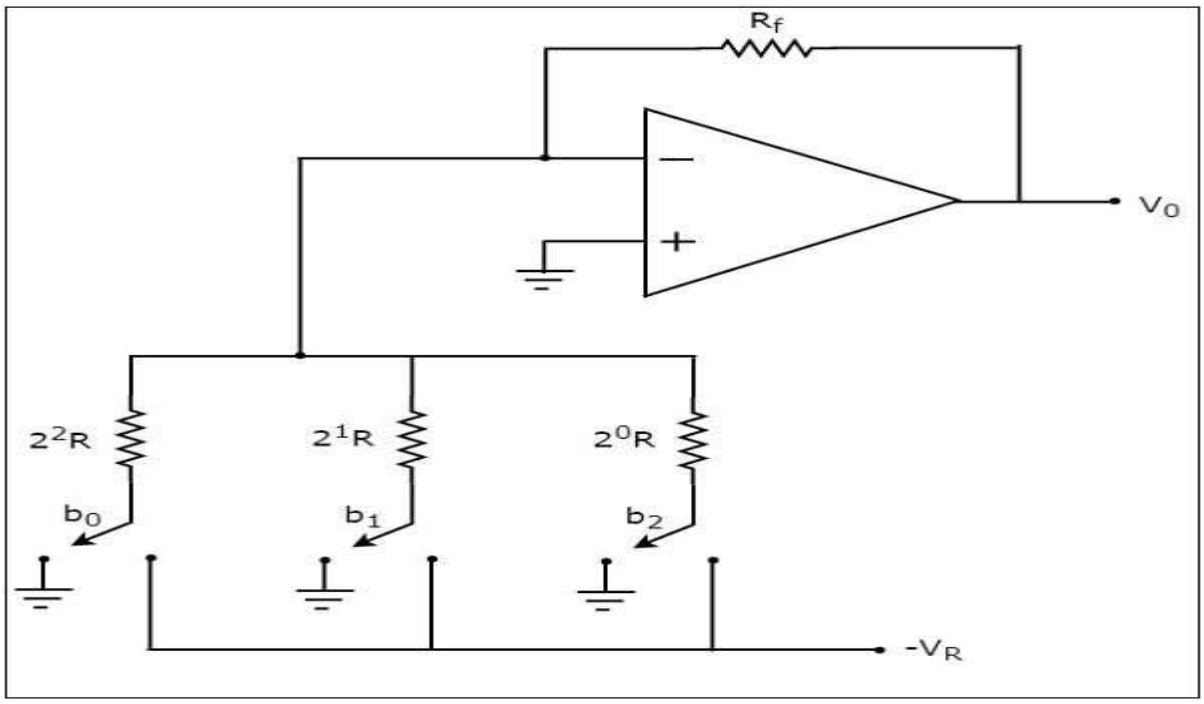
- Weighted Resistor DAC
- R-2R Ladder DAC

This section discusses about these two types of DACs in detail −

Weighted Resistor DAC:

A weighted resistor DAC produces an analog output, which is almost equal to the digital (binary) input by using **binary weighted resistors** in the inverting adder circuit. In short, a binary weighted resistor DAC is called as weighted resistor DAC.

The **circuit diagram** of a 3-bit binary weighted resistor DAC is shown below:



Recall that the bits of a binary number can have only one of the two values. i.e., either 0 or 1. Let the **3-bit binary input** is b2b1b0. Here, the bits b2 and b0 denote the **Most Significant Bit (MSB) and Least Significant Bit (LSB)** respectively.

The **digital switches** shown in the above figure will be connected to ground, when the corresponding input bits are equal to '0'. Similarly, the digital switches shown in the above figure will be connected to the negative reference voltage, −VR when the corresponding input bits are equal to '1'.

In the above circuit, the non-inverting input terminal of an op-amp is connected to ground. That means zero volts is applied at the non-inverting input terminal of op-amp.

According to the **virtual short concept**, the voltage at the inverting input terminal of opamp is same as that of the voltage present at its non-inverting input terminal. So, the voltage at the inverting input terminal's node will be zero volts.

The above equation represents the **output voltage equation** of a 3-bit binary weighted resistor DAC. Since the number of bits are three in the binary (digital) input, we will get seven possible values of output voltage by varying the binary input from 000 to 111 for a fixed reference voltage, VRVR.

We can write the **generalized output voltage equation** of an N-bit binary weighted resistor DAC as shown below based on the output voltage equation of a 3-bit binary weighted resistor DAC.

$$=>V0=VR_2\{bN-12^0+bN-22^1+....+b02^{N-1}\}$$

$$=>V0=VR_2\{bN-12^0+bN-22^1+....+b02^{N-1}\}$$

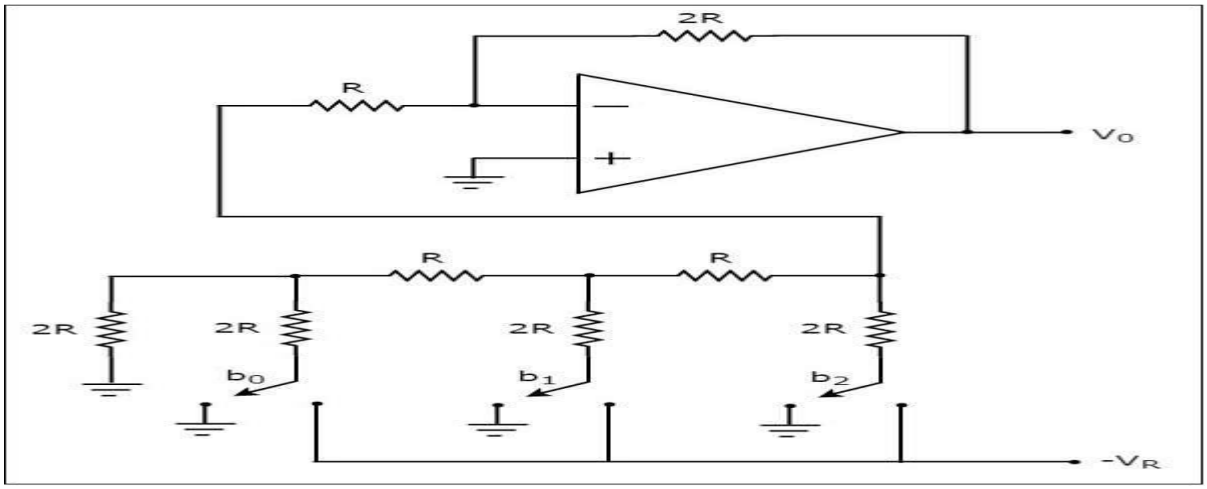
The **disadvantages** of a binary weighted resistor DAC are as follows −

- The difference between the resistance values corresponding to LSB & MSB will increase as the number of bits present in the digital input increases.
- It is difficult to design more accurate resistors as the number of bits present in the digital input increases.

R-2R Ladder DAC:

The R-2R Ladder DAC overcomes the disadvantages of a binary weighted resistor DAC. As the name suggests, R-2R Ladder DAC produces an analog output, which is almost equal to the digital (binary) input by using a **R-2R ladder network** in the inverting adder circuit.

The **circuit diagram** of a 3-bit R-2R Ladder DAC is shown in the following figure −



Recall that the bits of a binary number can have only one of the two values. i.e., either 0 or 1. Let the **3-bit binary input** is b2b1b0b2b1b0. Here, the bits b2b2 and b0b0 denote the Most Significant Bit (MSB) and Least Significant Bit (LSB) respectively.
The digital switches shown in the above figure will be connected to ground, when the corresponding input bits are equal to '0'. Similarly, the digital switches shown in above figure will be connected to the negative reference voltage, −VR−VR when the corresponding input bits are equal to '1'.

It is difficult to get the generalized output voltage equation of a R-2R Ladder DAC. But, we can find the analog output voltage values of R-2R Ladder DAC for individual binary input combinations easily.

The **advantages** of a R-2R Ladder DAC are as follows −

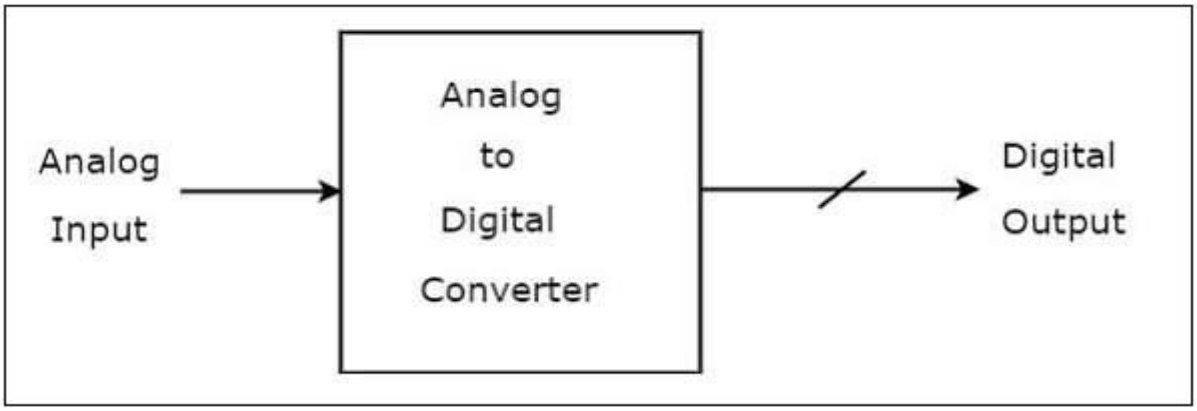
- R-2R Ladder DAC contains only two values of resistor: R and 2R. So, it is easy to select and design more accurate resistors.
- If more number of bits are present in the digital input, then we have to include required number of R-2R sections additionally.

Due to the above advantages, R-2R Ladder DAC is preferable over binary weighted resistor DAC.

Direct Type ADCs

An Analog to Digital Converter **(ADC)** converts an analog signal into a digital signal. The digital signal is represented with a binary code, which is a combination of bits 0 and 1.

The **block diagram** of an ADC is shown in the following figure −



Observe that in the figure shown above, an Analog to Digital Converter **(ADC)** consists of a single analog input and many binary outputs. In general, the number of binary outputs of ADC will be a power of two.

There are **two types** of ADCs: Direct type ADCs and Indirect type ADC. This chapter discusses about the Direct type ADCs in detail.

If the ADC performs the analog to digital conversion directly by utilizing the internally generated equivalent digital (binary) code for comparing with the analog input, then it is called as **Direct type ADC**.

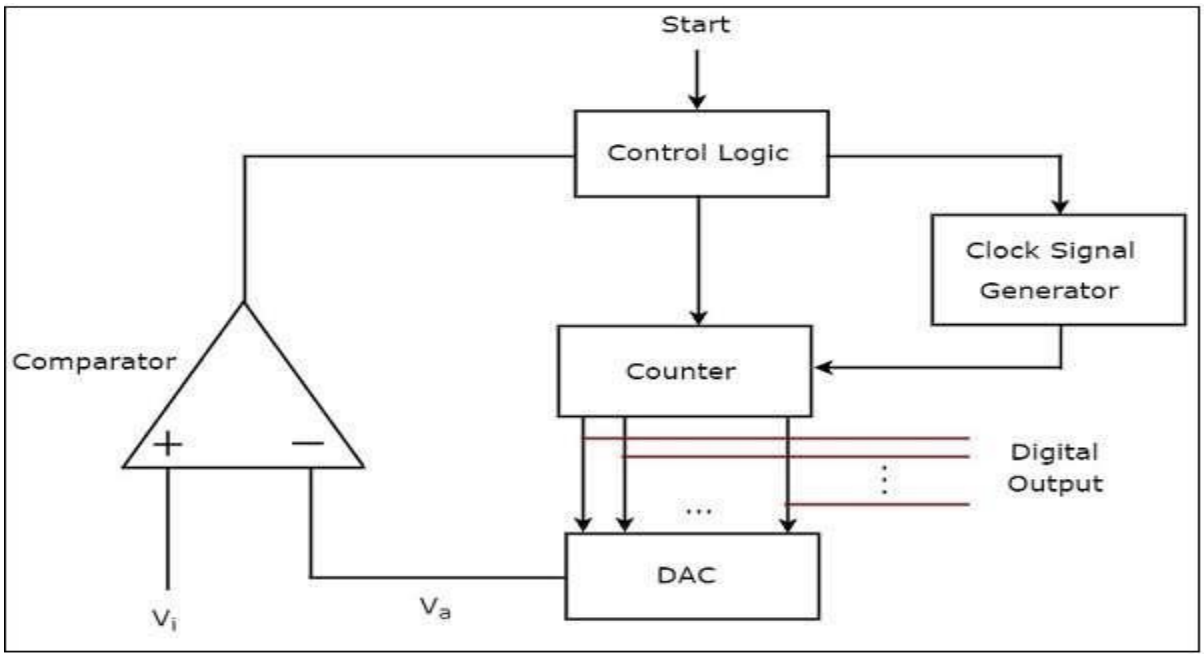
The following are the **examples** of Direct type ADCs −

- Counter type ADC
- Successive Approximation ADC
- Flash type ADC

Counter type ADC:

A **counter type ADC** produces a digital output, which is approximately equal to the analog input by using counter operation internally.

The **block diagram** of a counter type ADC is shown in the following figure −



The counter type ADC mainly consists of 5 blocks: Clock signal generator, Counter, DAC, Comparator and Control logic.

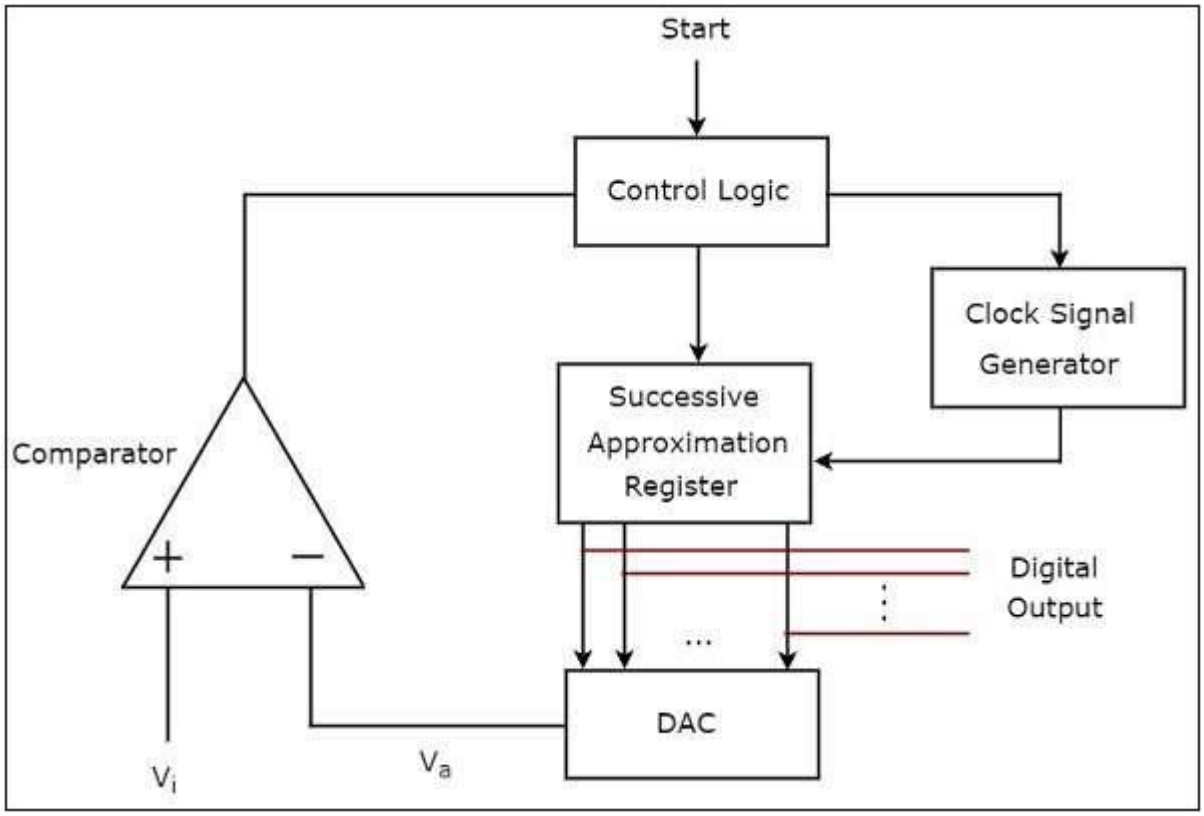
The **working** of a counter type ADC is as follows −

- The **control logic** resets the counter and enables the clock signal generator in order to send the clock pulses to the counter, when it received the start commanding signal.
- The **counter** gets incremented by one for every clock pulse and its value will be in binary (digital) format. This output of the counter is applied as an input of DAC.
- **DAC** converts the received binary (digital) input, which is the output of counter, into an analog output. Comparator compares this analog value,VaVa with the external analog input value Vi.
- The **output of comparator** will be **'1'** as long as Vi is greater than. The operations mentioned in above two steps will be continued as long as the control logic receives '1' from the output of comparator.
- The **output of comparator** will be **'0'** when Vi is less than or equal to Va. So, the control logic receives '0' from the output of comparator. Then, the control logic disables the clock signal generator so that it doesn't send any clock pulse to the counter.
- At this instant, the output of the counter will be displayed as the **digital output**. It is almost equivalent to the corresponding external analog input value Vi.

Successive Approximation ADC:

A **successive approximation type ADC** produces a digital output, which is approximately equal to the analog input by using successive approximation technique internally.

The **block diagram** of a successive approximation ADC is shown in the following figure



The successive approximation ADC mainly consists of 5 blocks− Clock signal generator, Successive Approximation Register (SAR), DAC, comparator and Control logic.

The **working** of a successive approximation ADC is as follows −

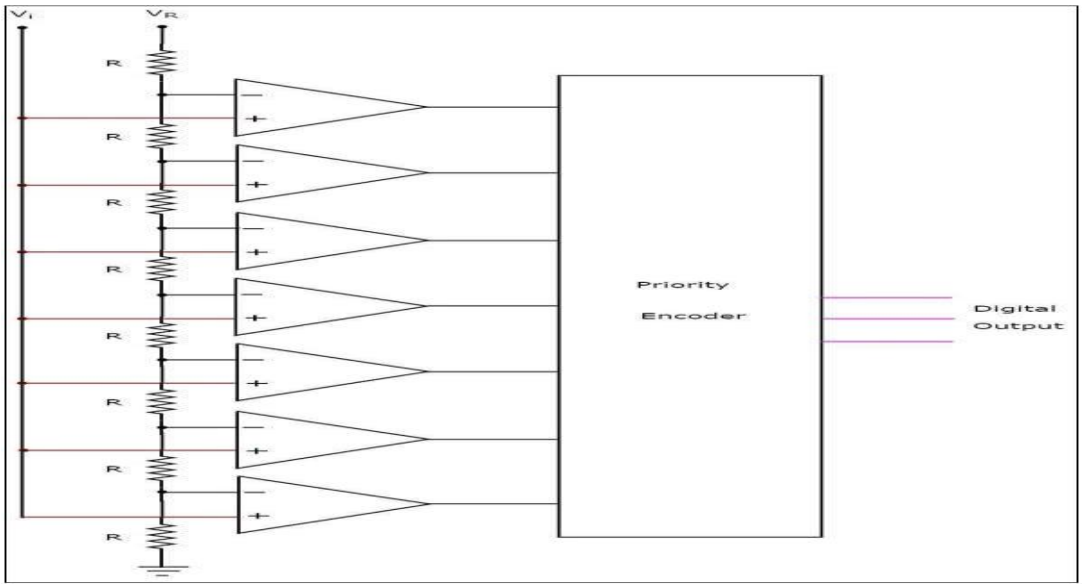
- The **control logic** resets all the bits of SAR and enables the clock signal generator in order to send the clock pulses to SAR, when it received the start commanding signal.
- The binary (digital) data present in **SAR** will be updated for every clock pulse based on the output of comparator. The output of SAR is applied as an input of DAC.
- **DAC** converts the received digital input, which is the output of SAR, into an analog output. The comparator compares this analog value VaVa with the external analog input value ViVi.
- The **output of a comparator** will be '1' as long as ViVi is greater than VaVa. Similarly, the output of comparator will be '0', when ViVi is less than or equal to VaVa.
- The operations mentioned in above steps will be continued until the digital output is a valid one.

The digital output will be a valid one, when it is almost equivalent to the corresponding external analog input value ViVi.

Flash type ADC:

A **flash type ADC** produces an equivalent digital output for a corresponding analog input in no time. Hence, flash type ADC is the fastest ADC.

The **circuit diagram** of a 3-bit flash type ADC is shown in the following figure −



The 3-bit flash type ADC consists of a voltage divider network, 7 comparators and a priority encoder.

The **working** of a 3-bit flash type ADC is as follows.

- The **voltage divider network** contains 8 equal resistors. A reference voltage VRVR is applied across that entire network with respect to the ground. The voltage drop across each resistor from bottom to top with respect to ground will be the integer multiples (from 1 to 8) of VR8.
- The external **input voltage** ViVi is applied to the non-inverting terminal of all comparators. The voltage drop across each resistor from bottom to top with respect to ground is applied to the inverting terminal of comparators from bottom to top.
- At a time, all the comparators compare the external input voltage with the voltage drops present at the respective other input terminal. That means, the comparison operations take place by each comparator **parallelly**.
- The **output of the comparator** will be '1' as long as ViVi is greater than the voltage drop present at the respective other input terminal. Similarly, the output of comparator will be '0', when, ViVi is less than or equal to the voltage drop present at the respective other input terminal.
- All the outputs of comparators are connected as the inputs of **priority encoder**.This priority encoder produces a binary code (digital output), which is corresponding to the high priority input that has '1'.
- Therefore, the output of priority encoder is nothing but the binary equivalent **(digital output)** of external analog input voltage, ViVi.

The flash type ADC is used in the applications where the conversion speed of analog input into digital data should be very high.

MODULE-V

Basic Structure of CMOS Logic Gate Circuits

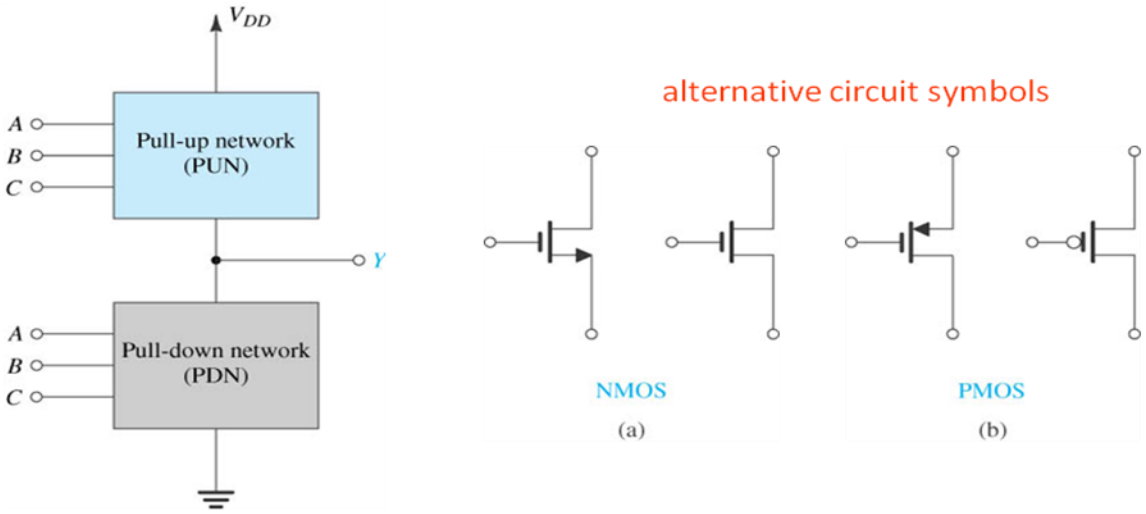


Figure 10.8 Representation of a three-input CMOS logic gate. The PUN comprises PMOS transistors, and the PDN comprises NMOS transistors.

Basic Structure of CMOS Logic Gate Circuits

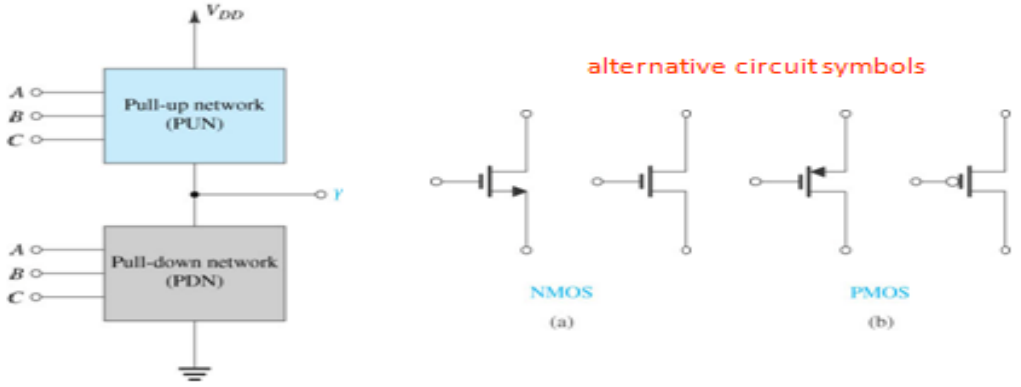
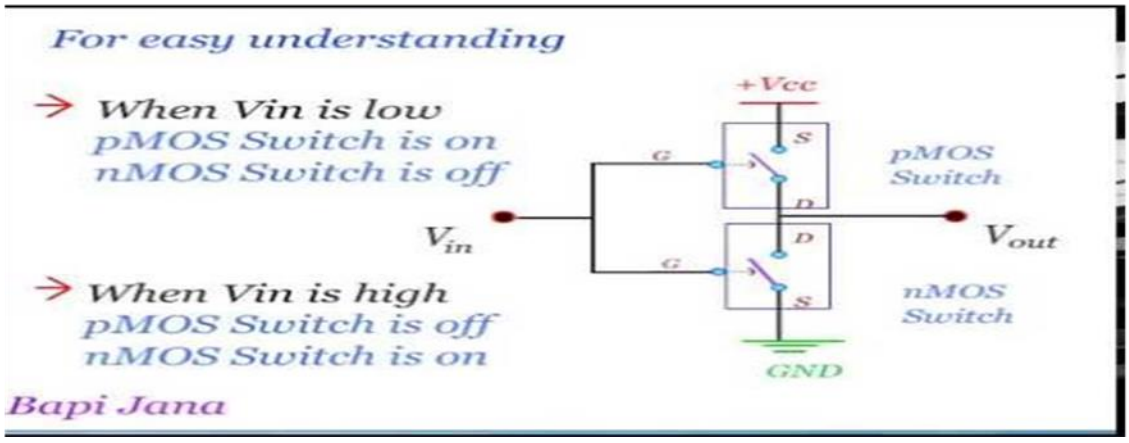


Figure 10.8 Representation of a three-input CMOS logic gate. The PUN comprises PMOS transistors, and the PDN comprises NMOS transistors.

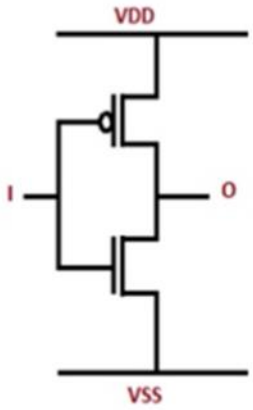
Working of CMOS Inverter



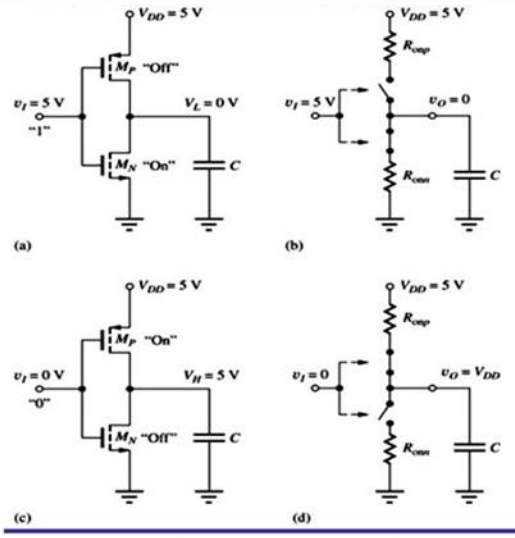
Basic Working Principle

The CMOS Inverter

- The inverter circuit as shown in the figure consists of two complementary MOSFETs pmos and nmos. The input I serves as the gate voltage for both the transistors.
- The nmos transistor has an input from vss or ground (in most cases) and the pmos transistor has an input from vdd. The terminal 'O' serves as the output for both pmos and nmos.
- When a high voltage(~vdd) is given at I, the nmos is turned-on while the pmos is switched-off. The output is 'pulled-down' to vss.
- Similarly, when a low gate-voltage I (~0) is applied, the nmos is switched-off while the pmos is switched-on. The output in this case becomes vdd or the output is 'pulled-up' to vdd

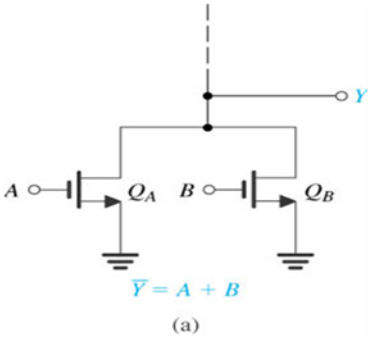


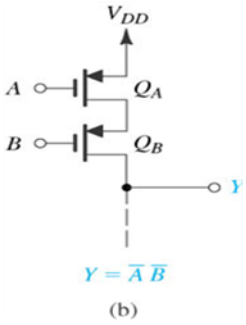
Static Characteristics of the CMOS Inverter



- The figure shows the two modes of static operation with the circuit and simplified models
- Notice that $V_H = 5V$ and $V_L = 0V$, and that $I_D = 0A$ which means that there is no static power dissipation

CMOS NOR Gate





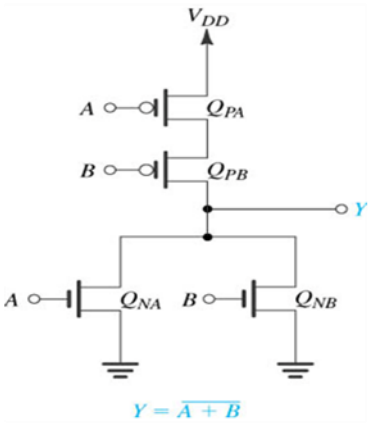


Figure 10.12 A two-input CMOS NOR gate.

CMOS NAND Gate

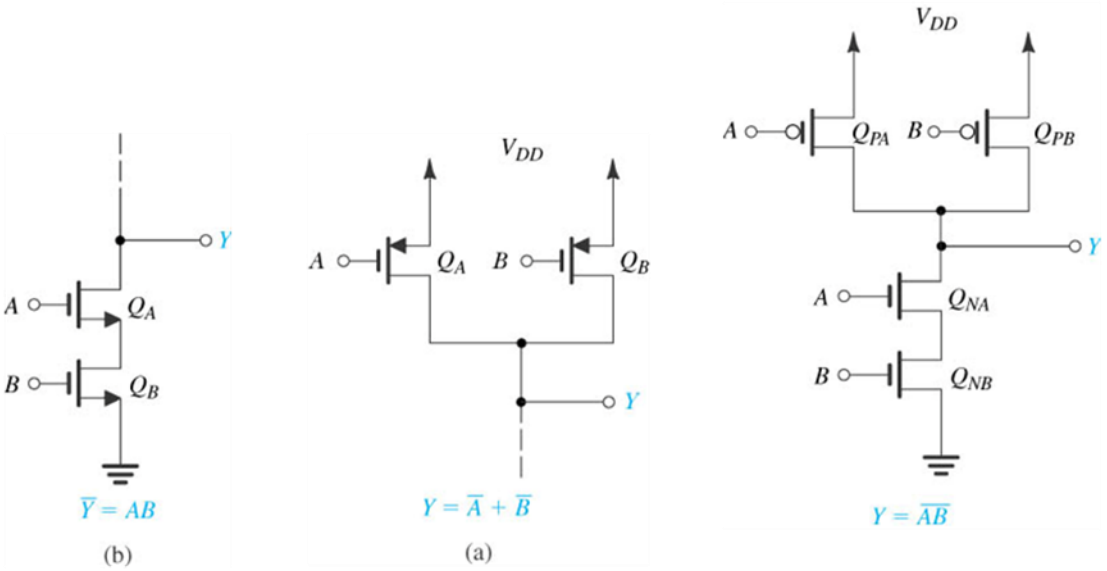


Figure 10.13 A two-input CMOS NAND gate.

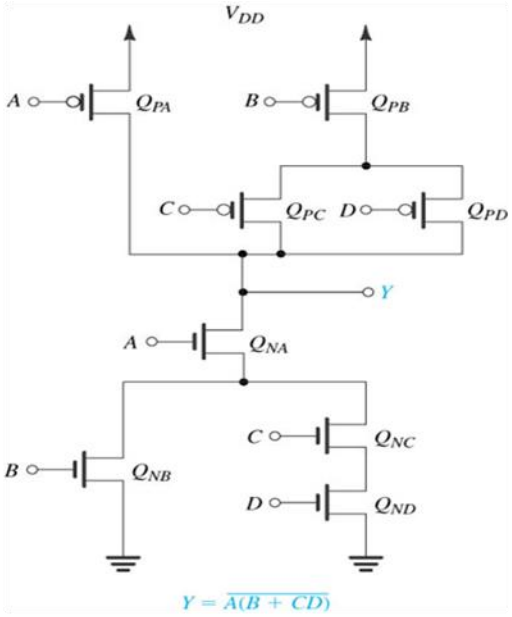
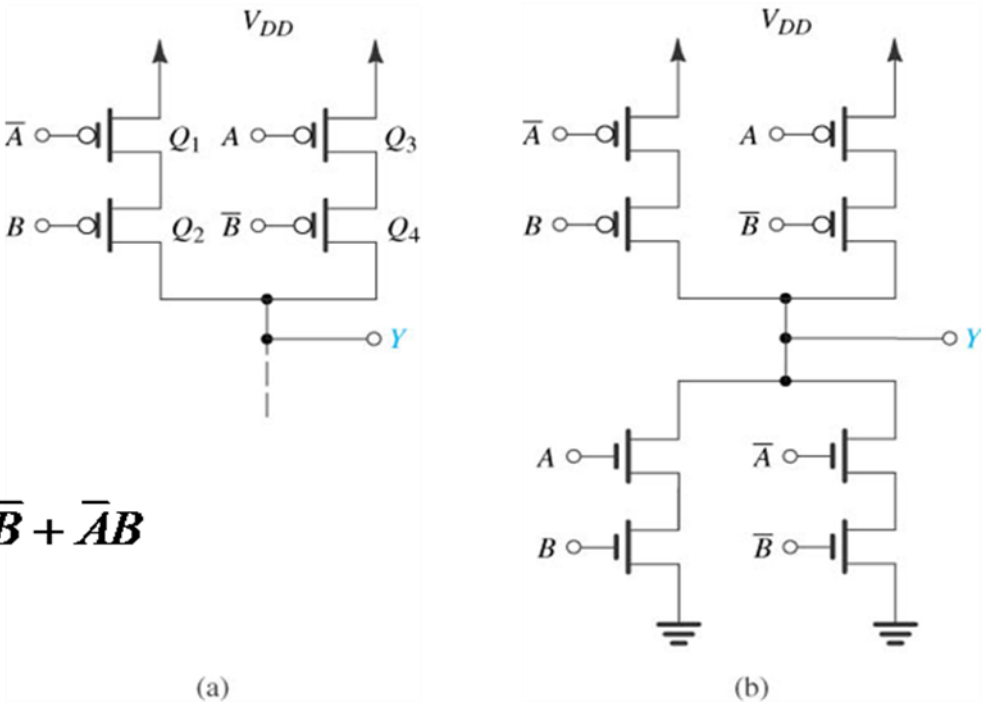


Figure 10.14 CMOS realization of a complex gate.

CMOS XOR Gate



$$Y = A\overline{B} + \overline{A}B$$

Transistor Sizing

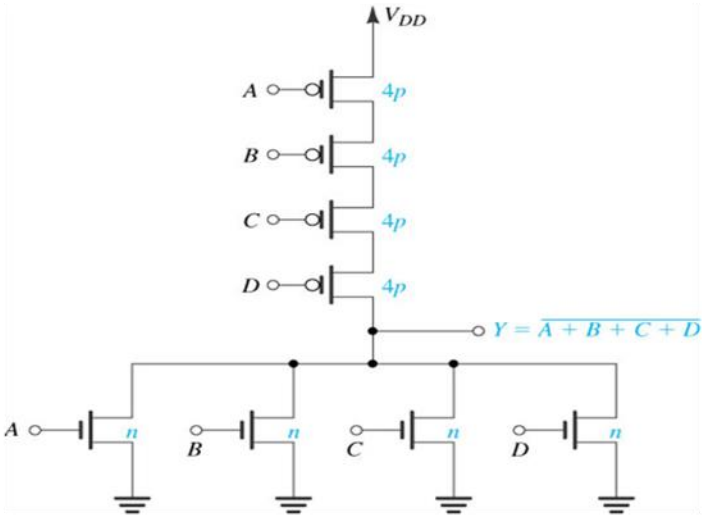


Figure 10.16 Proper transistor sizing for a four-input NOR gate. Note that n and p denote the (W/L) ratios of Q_N and Q_P, respectively, of the basic inverter.

COMBINATIONAL CIRCUITS USING TTL *74XX* ICS

- Study of logic gates using *74XX* ICs,
- Four-bit parallel adder(IC7483),
- Comparator(IC 7485),
- Decoder(IC 74138, IC 74154),
- BCD-to-7-segment decoder(IC 7447),
- Encoder(IC 74147),
- Multiplexer(IC74151),
- Demultiplexer (IC 74154).

IC 7483 – internal architecture

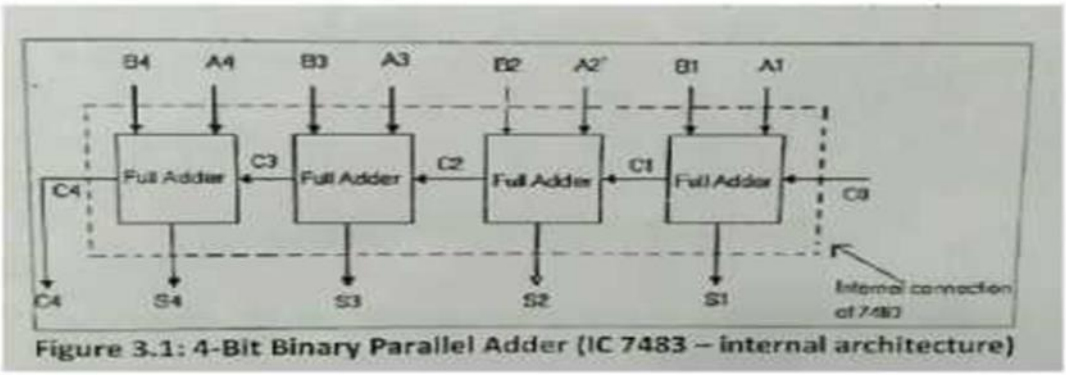


Figure 3.1: 4-Bit Binary Parallel Adder (IC 7483 – internal architecture)

PIN DIAGRAM

4-Bit Binary Parallel Adder

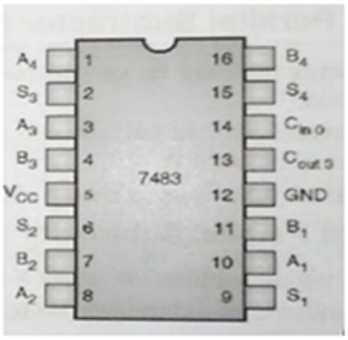
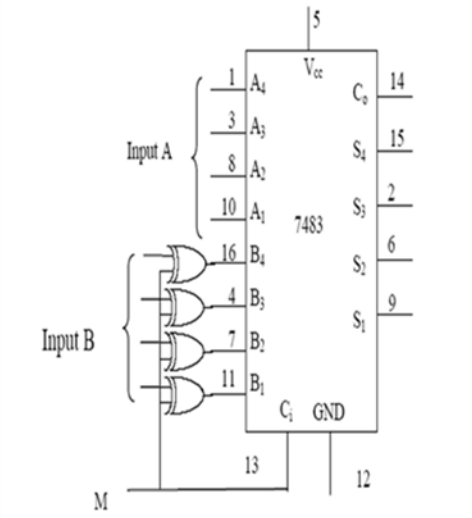


Fig1. Pin diagram of IC 7483



8-bit parallel adder using two IC7483

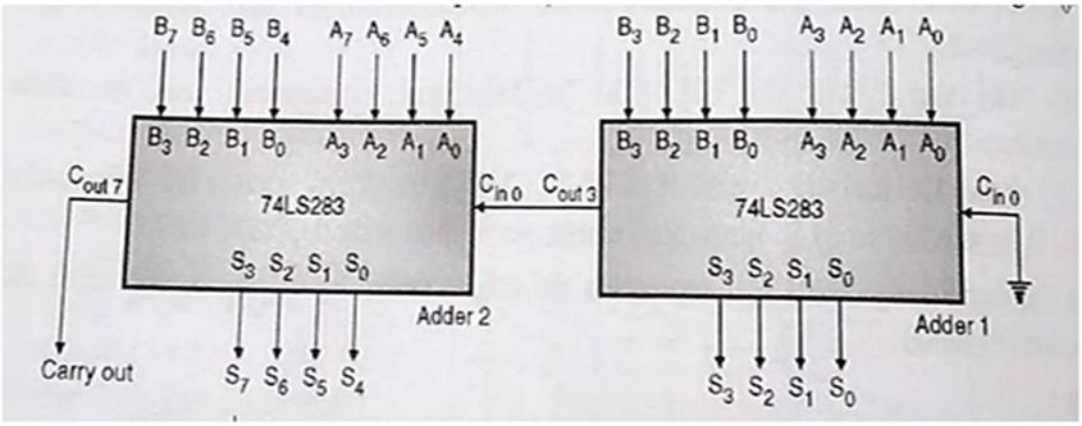
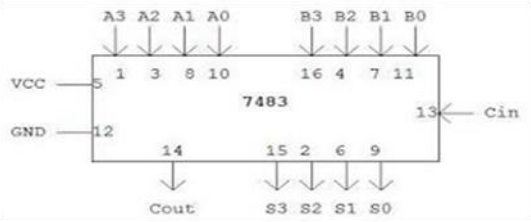
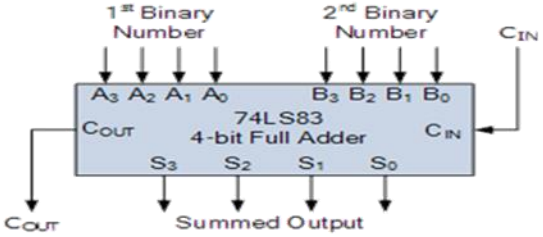


Fig2. Cascading of two IC 7483s

Block Diagram Representation





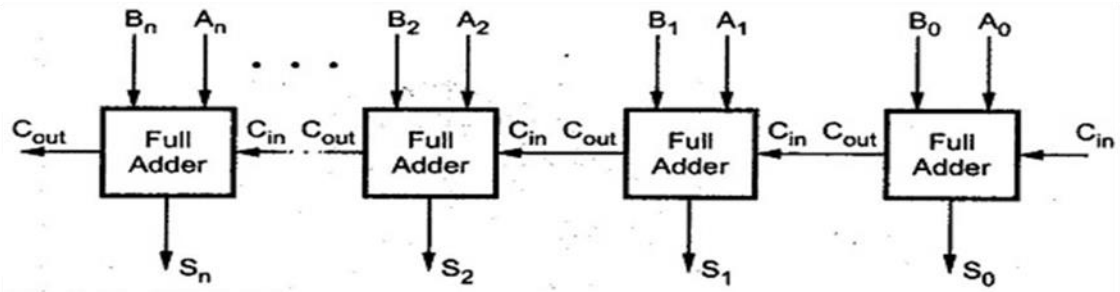
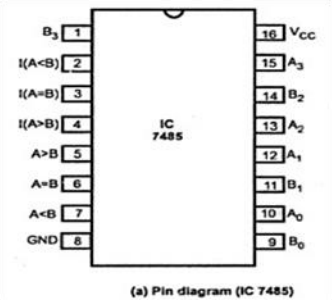


Fig. 3.25 Block diagram of n-bit parallel adder

Pin Diagram & Logic Diagram

4-Bit Comparator



(a) Pin diagram (IC 7485)

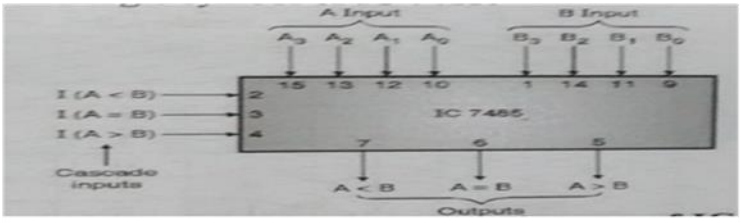
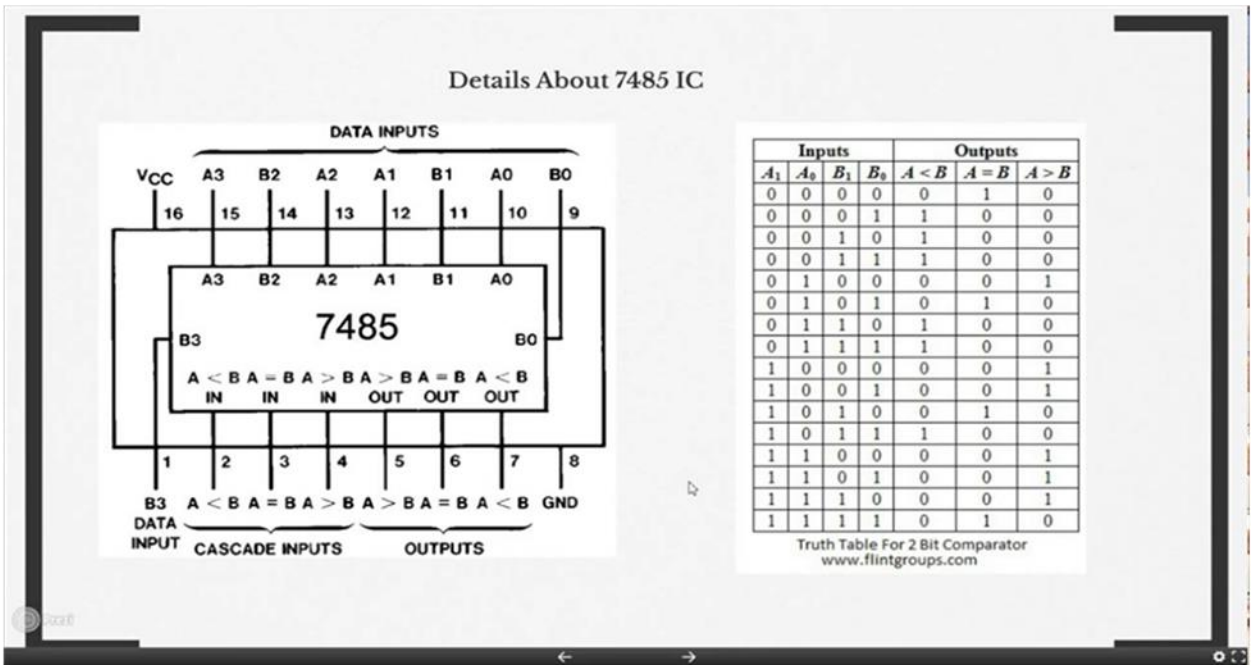


Fig13. Logic diagram of IC7485

Truth Table



Inputs				Outputs		
A_1	A_0	B_1	B_0	$A<B$	$A=B$	$A>B$
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

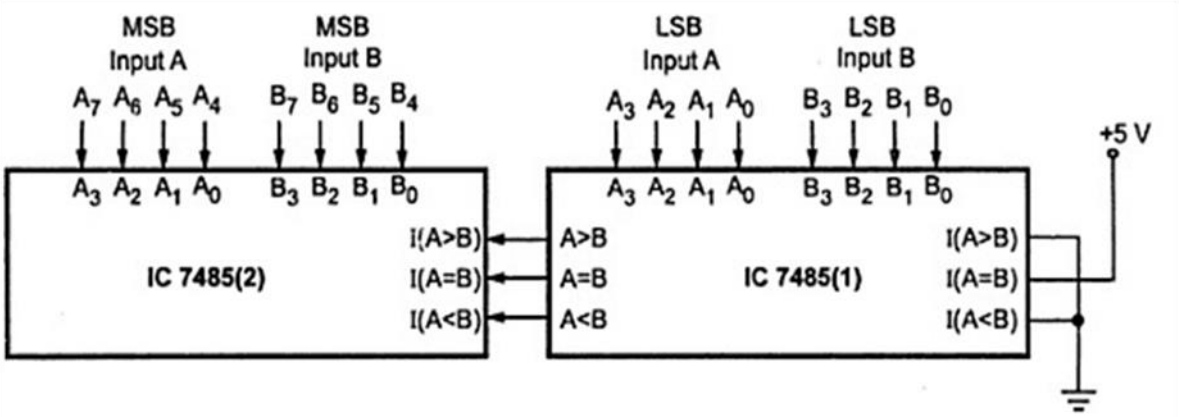
Truth Table of 4Bit Comparator

Table 10.1 Truth table of 7485

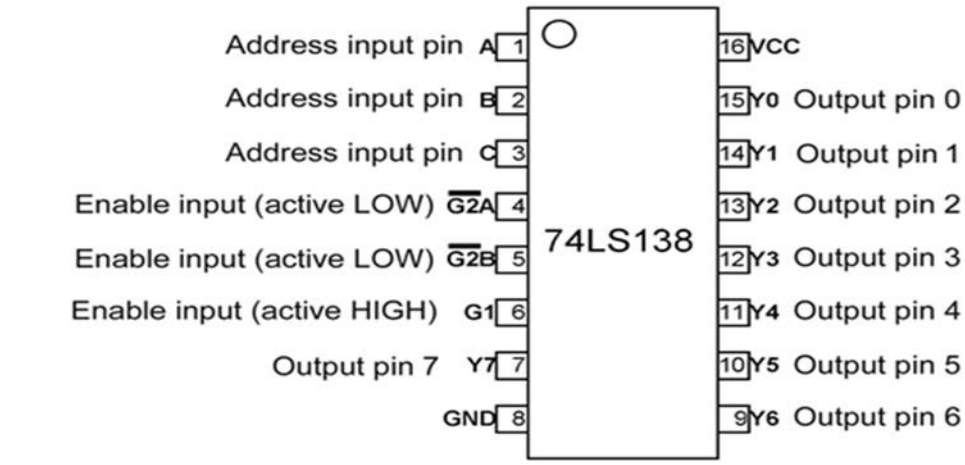
Comparing inputs								Cascading inputs			Outputs		
A_3,	B_3	A_2,	B_2	A_1,	B_1	A_0,	B_0	$A>B$	$A<B$	$A=B$	$A>B$	$A<B$	$A=B$
$A_3 > B_3$		×		×		×		×	×	×	1	0	0
$A_3 < B_3$		×		×		×		×	×	×	0	1	0
$A_3 = B_3$		$A_2 > B_2$		×		×		×	×	×	1	0	0
$A_3 = B_3$		$A_2 < B_2$		×		×		×	×	×	0	1	0
$A_3 = B_3$		$A_2 = B_2$		$A_1 > B_1$		×		×	×	×	1	0	0
$A_3 = B_3$		$A_2 = B_2$		$A_1 < B_1$		×		×	×	×	0	1	0
$A_3 = B_3$		$A_2 = B_2$		$A_1 = B_1$		$A_0 > B_0$		×	×	×	1	0	0
$A_3 = B_3$		$A_2 = B_2$		$A_1 = B_1$		$A_0 < B_0$		×	×	×	0	1	0
$A_3 = B_3$		$A_2 = B_2$		$A_1 = B_1$		$A_0 = B_0$		1	0	0	1	0	0
$A_3 = B_3$		$A_2 = B_2$		$A_1 = B_1$		$A_0 = B_0$		0	1	0	0	1	0
$A_3 = B_3$		$A_2 = B_2$		$A_1 = B_1$		$A_0 = B_0$		0	0	1	0	0	1
$A_3 = B_3$		$A_2 = B_2$		$A_1 = B_1$		$A_0 = B_0$		×	×	1	0	0	1
$A_3 = B_3$		$A_2 = B_2$		$A_1 = B_1$		$A_0 = B_0$		1	1	0	0	0	0
$A_3 = B_3$		$A_2 = B_2$		$A_1 = B_1$		$A_0 = B_0$		0	0	0	1	1	0

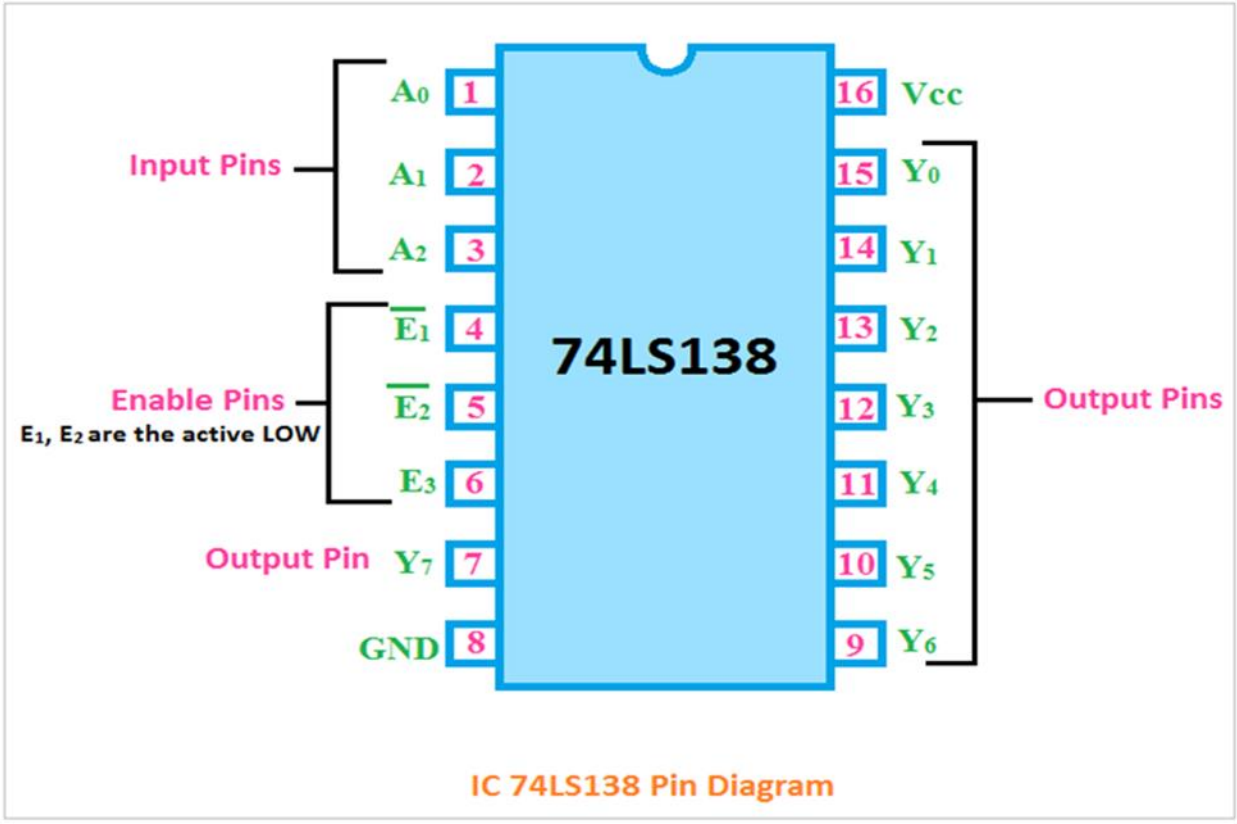
Cascading of two Comparators

8 Bit Comparator using two 4-bit Comparators



3x8 Decoder (IC74138)



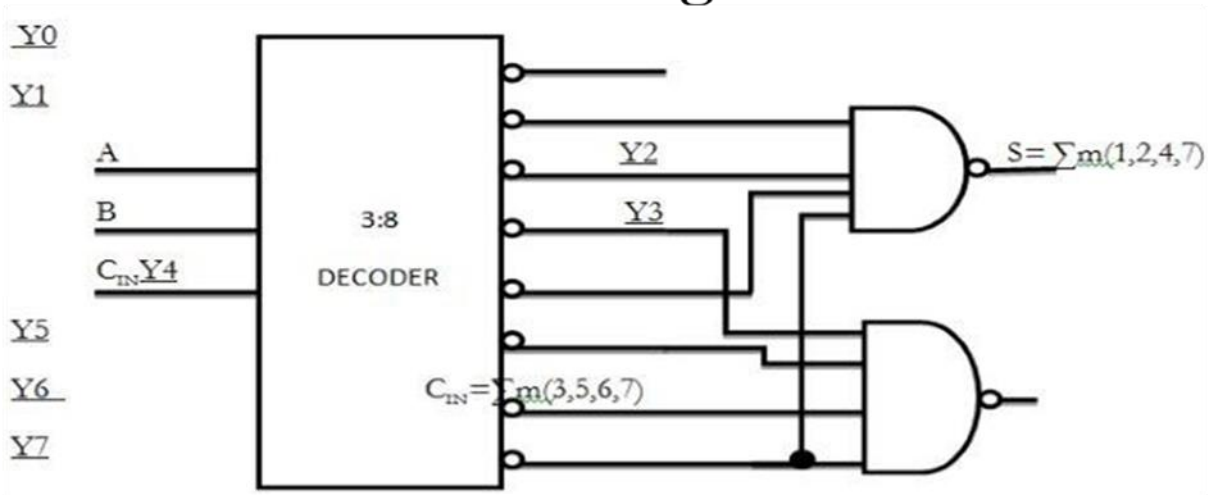


IC 74LS138 Pin Diagram

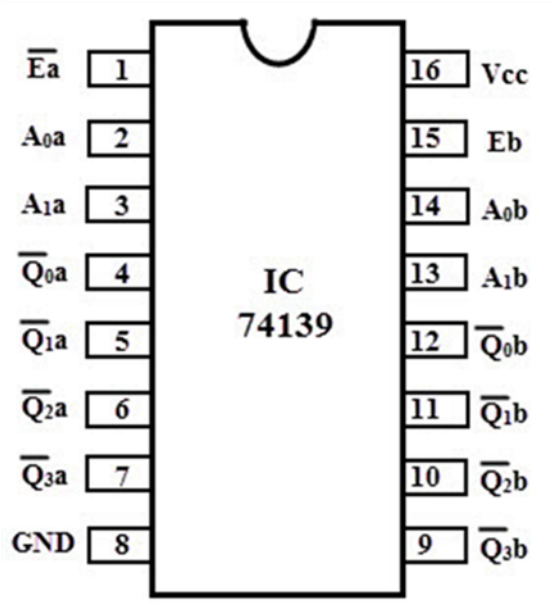
Truth Table

Input						Output							
E1	E2	E3	A0	A1	A2	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

Full Adder using IC74138



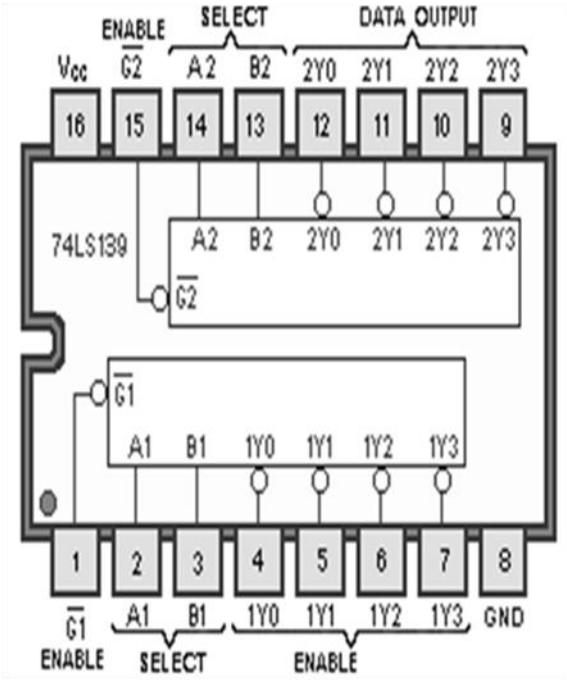
Dual 2x4 Decoder (IC74139)



FUNCTION TABLE

INPUTS			OUTPUTS			
$\overline{G}$	SELECT					
	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

Pin Diagram



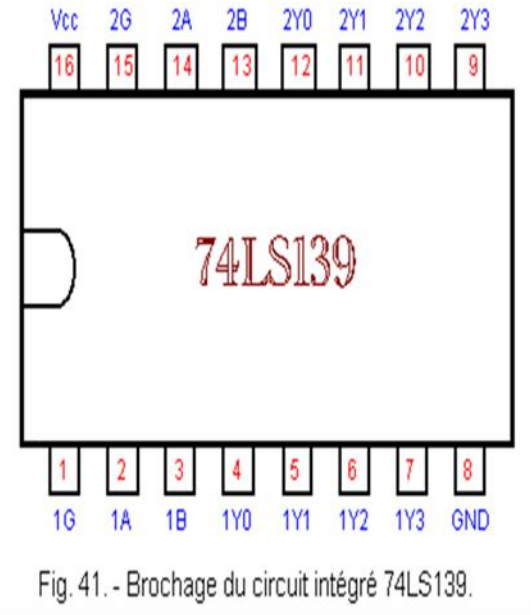


Fig. 41. - Brochage du circuit intégré 74LS139.

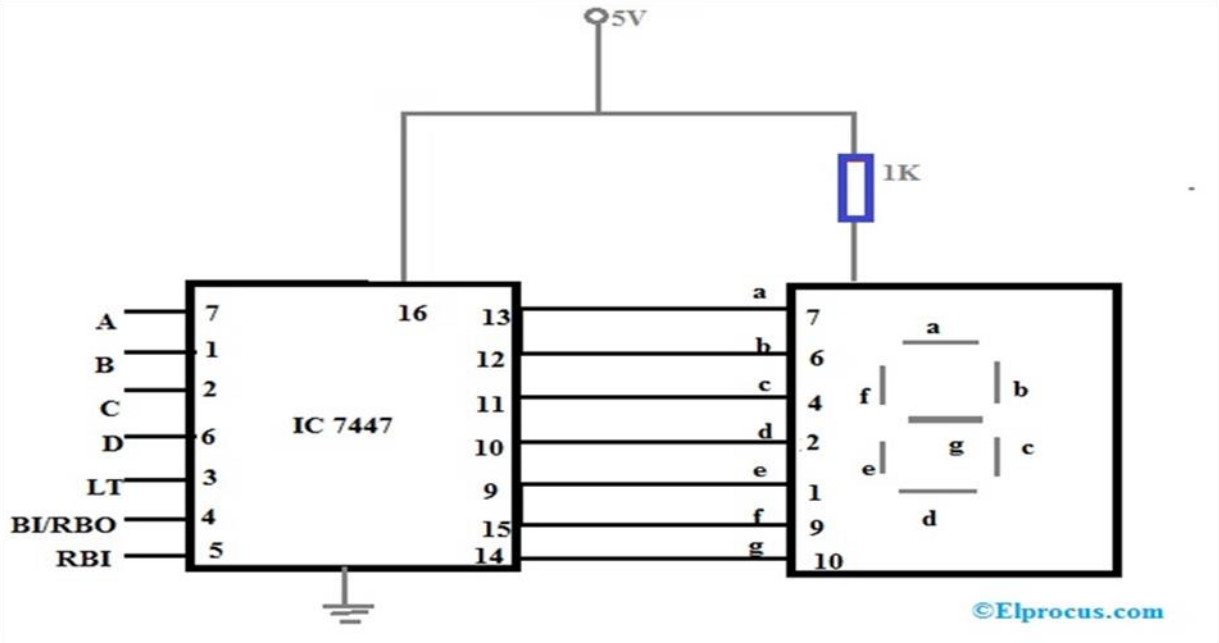
Truth table

Function Table

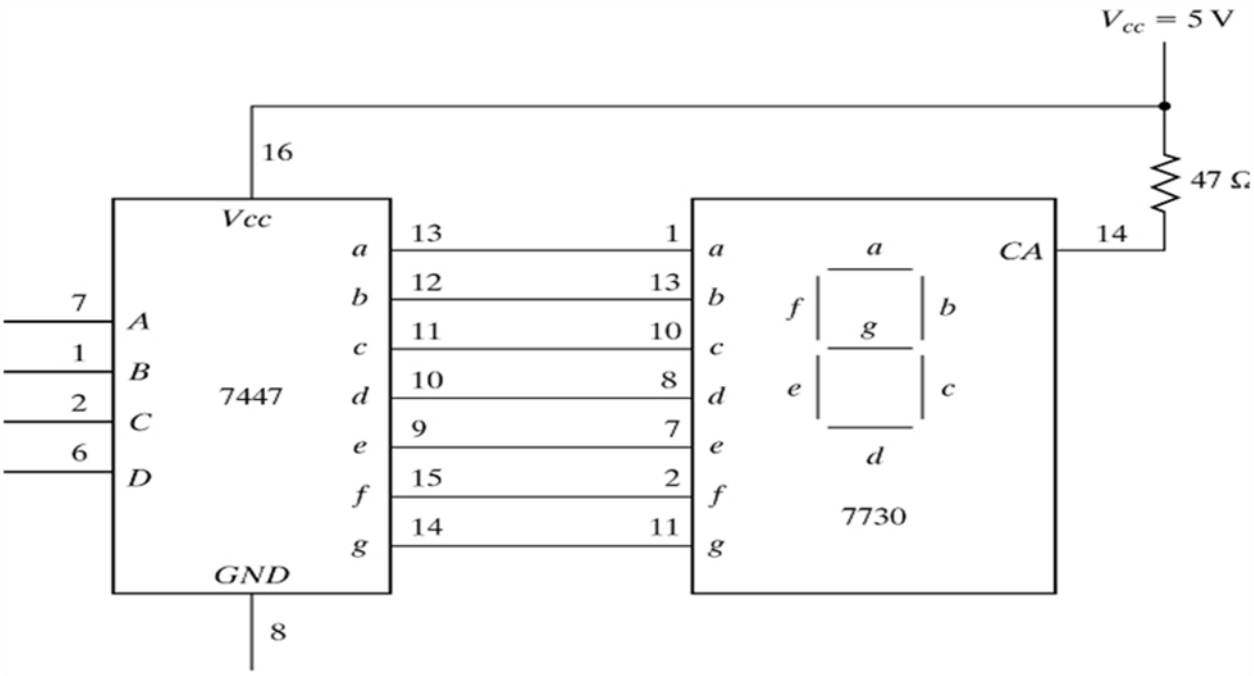
Inputs						Outputs															
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level, L = Low Level, X = Don't Care

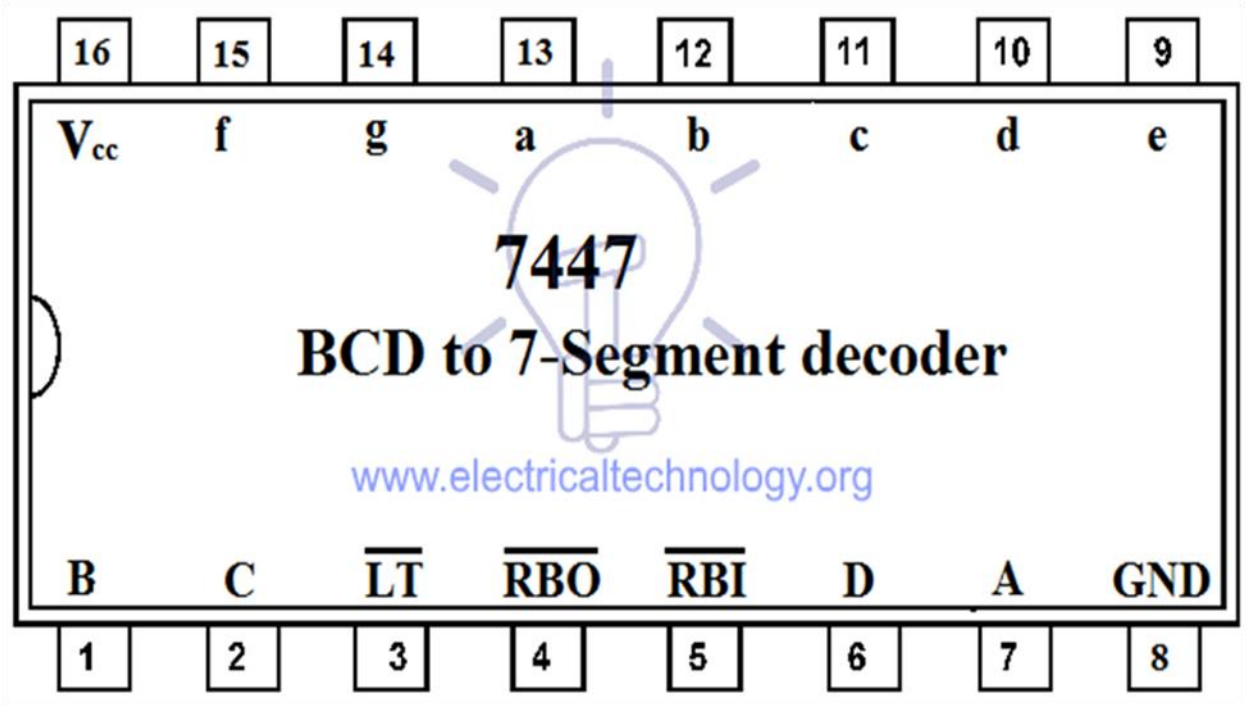
BCD-to-7-segment decoder(IC 7447)



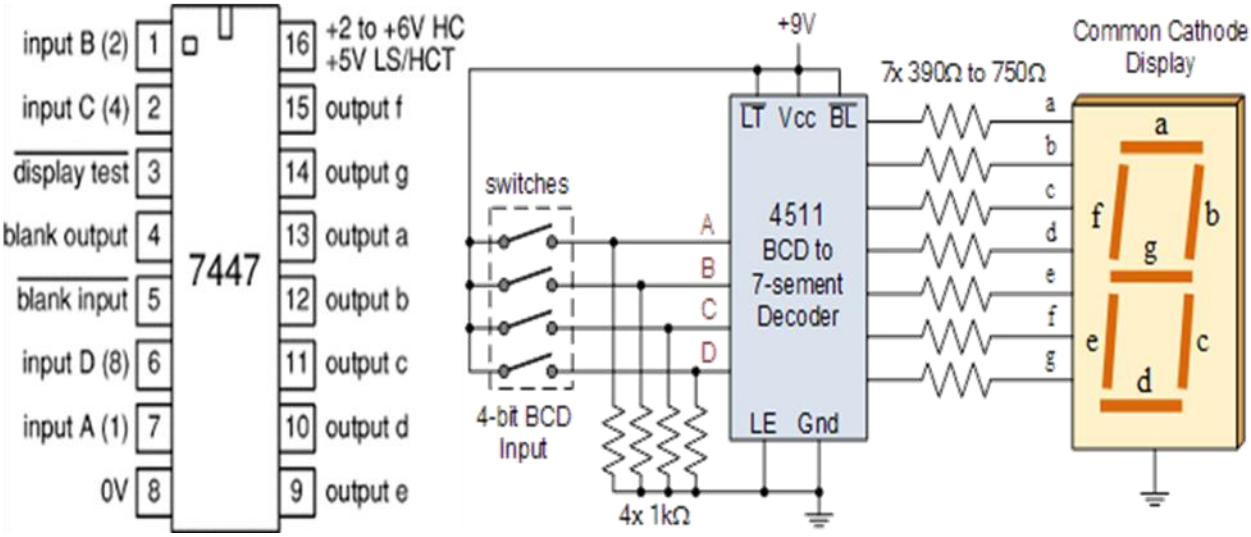
BCD to 7-Segment Display



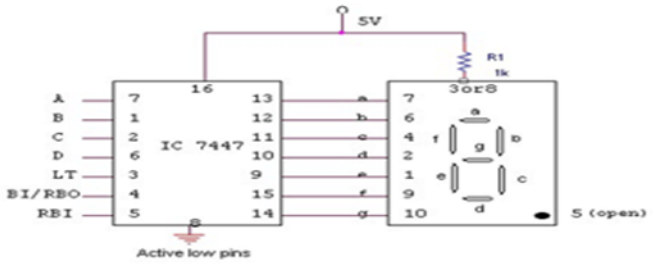
Pin Diagram



Pin Diagram



Truth Table

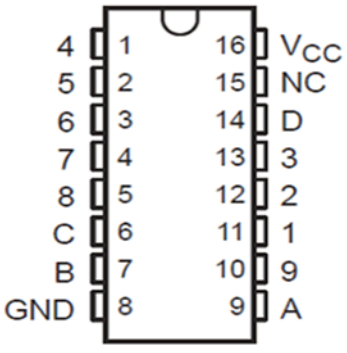


TRUTH TABLE:

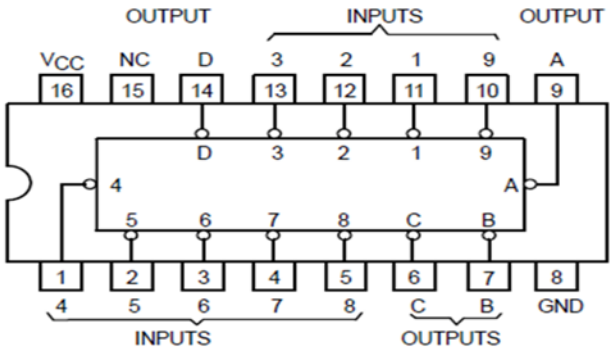
BCD Inputs				Output Logic Levels from IC 7447 to 7-segments							Decimal number display
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	1	0	0	1	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0	2
0	0	1	1	0	0	0	0	1	1	0	3
0	1	0	0	1	0	0	1	1	0	0	4
0	1	0	1	0	1	0	0	1	0	0	5
0	1	1	0	1	1	0	0	0	0	0	6
0	1	1	1	0	0	0	1	1	1	1	7
1	0	0	0	0	0	0	0	0	0	0	8
1	0	0	1	0	0	0	1	1	0	0	9

Priority Encoder

74147



74LS147



Decimal to BCD Encoder

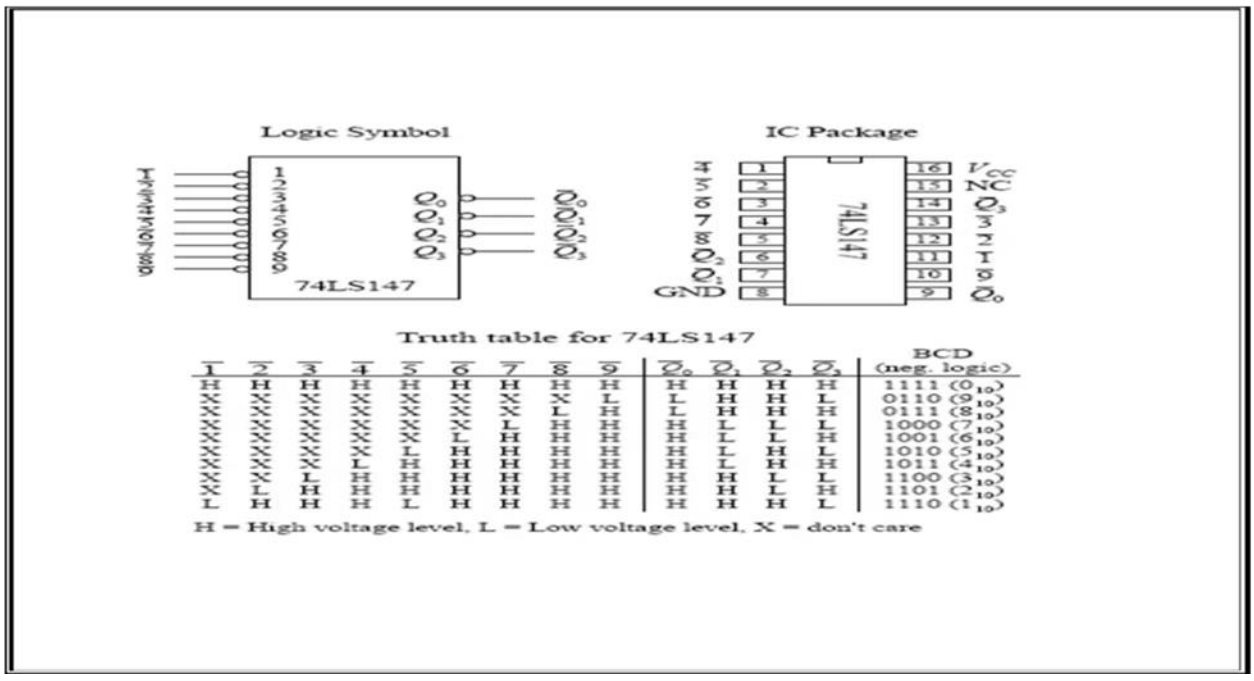
74147 Truth Table

FUNCTION TABLE – '147, 'LS147

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = high logic level, L = low logic level, X = irrelevant

Decimal to BCD Encoder



Truth table for 74LS147

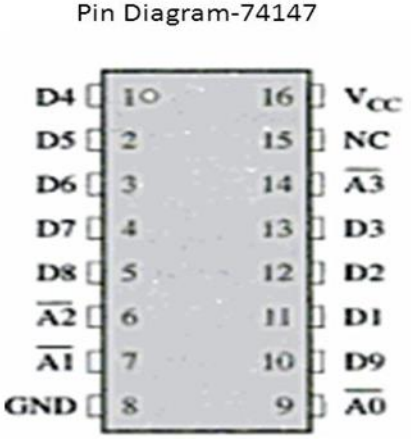
$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$	$\overline{8}$	$\overline{9}$	$\overline{D}_0$	$\overline{D}_1$	$\overline{D}_2$	$\overline{D}_3$	BCD (neg. logic)
H	H	H	H	H	H	H	H	H	H	H	H	H	1111 (0_{10})
X	X	X	X	X	X	X	X	L	L	H	H	L	0110 (9_{10})
X	X	X	X	X	X	X	L	H	L	H	H	L	0111 (8_{10})
X	X	X	X	X	X	L	H	H	H	L	L	H	1000 (7_{10})
X	X	X	X	X	L	H	H	H	H	L	L	L	1001 (6_{10})
X	X	X	X	L	H	H	H	H	H	L	H	H	1010 (5_{10})
X	X	X	L	H	H	H	H	H	H	L	H	L	1011 (4_{10})
X	X	L	H	H	H	H	H	H	H	H	L	H	1100 (3_{10})
X	L	H	H	H	H	H	H	H	H	H	L	L	1101 (2_{10})
L	H	H	H	L	H	H	H	H	H	H	H	L	1110 (1_{10})

H = High voltage level, L = Low voltage level, X = don't care

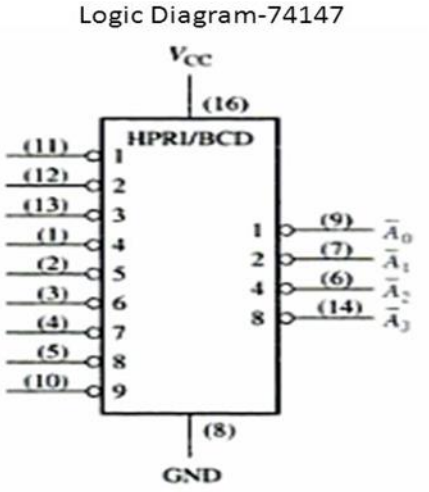
74HC147- priority encoder

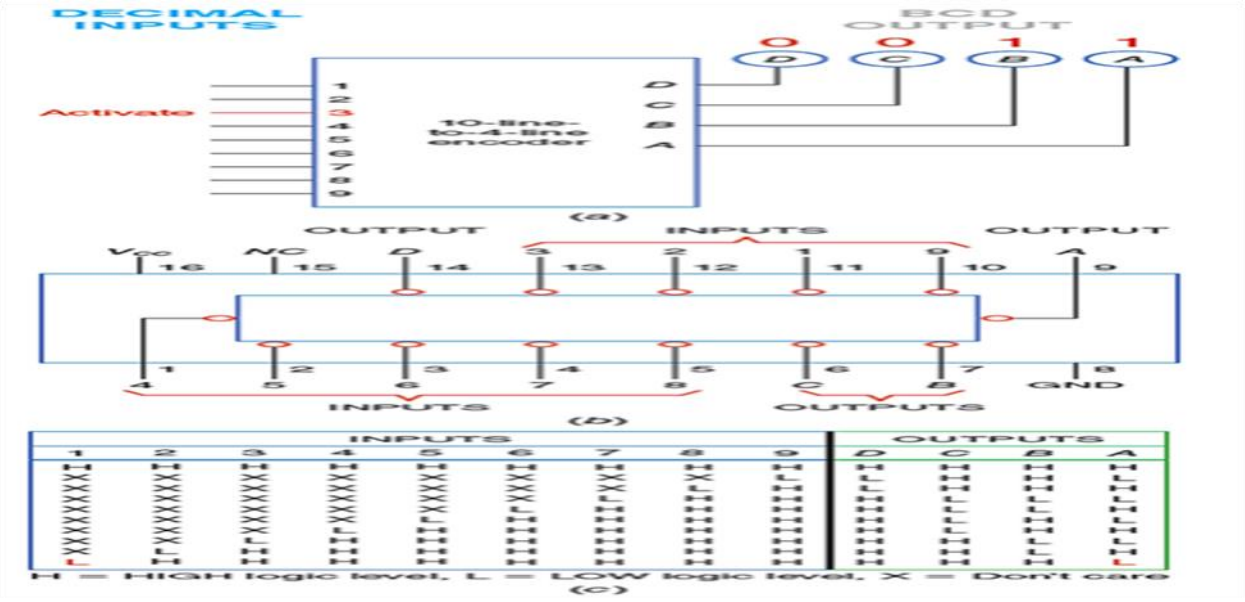
- It is also called as 10-line-to-4-line encoder.
- 74HC147 is a priority encoder with active-low inputs (0) for decimal digits 1 to 9 and active-low BCD outputs.

Pin Diagram-74147



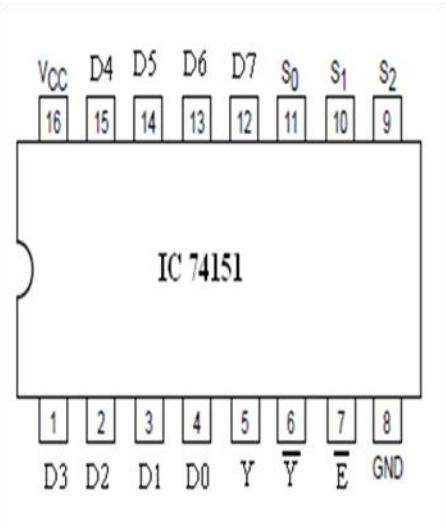
Logic Diagram-74147

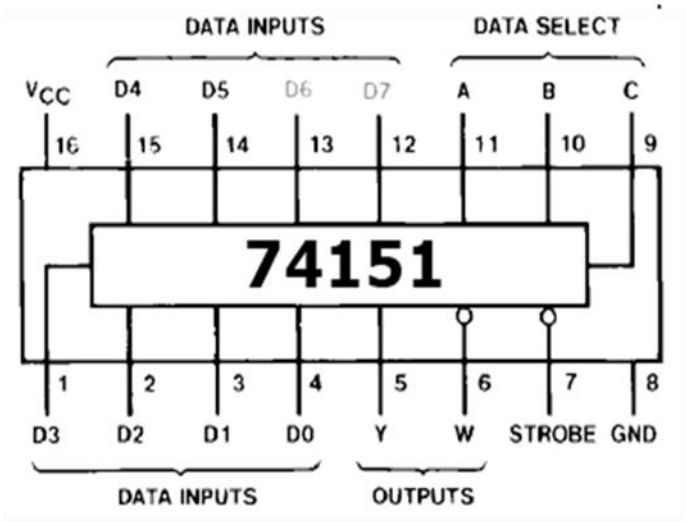




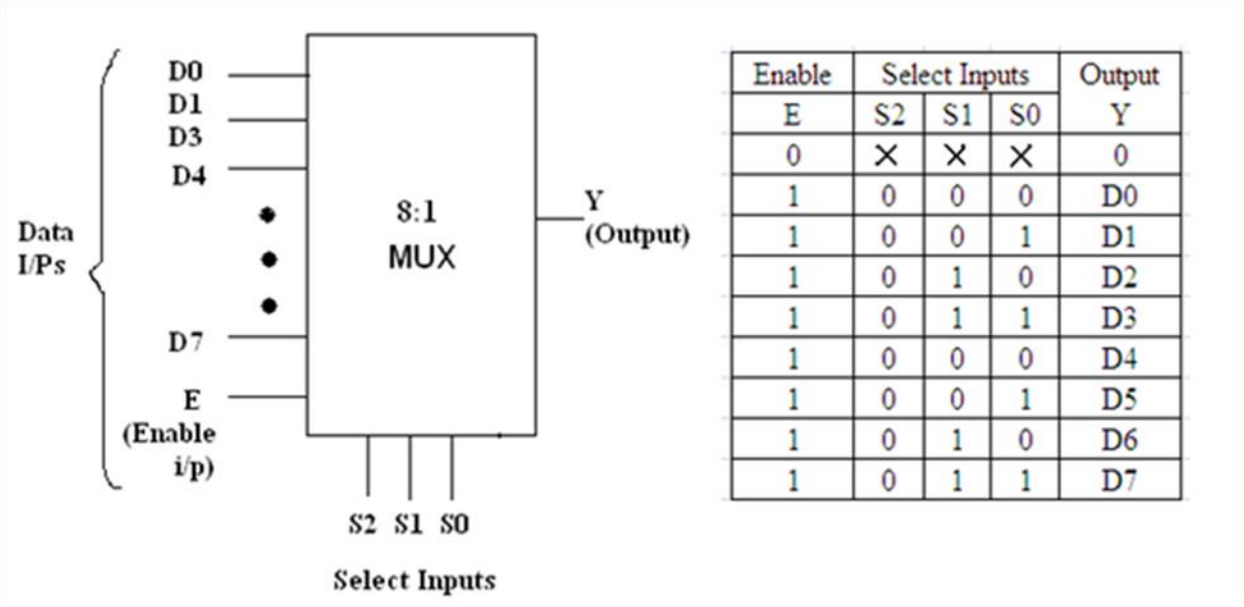
8x1 Multiplexer (IC74151)

Pin Diagram





Logic Diagram & Truth Table

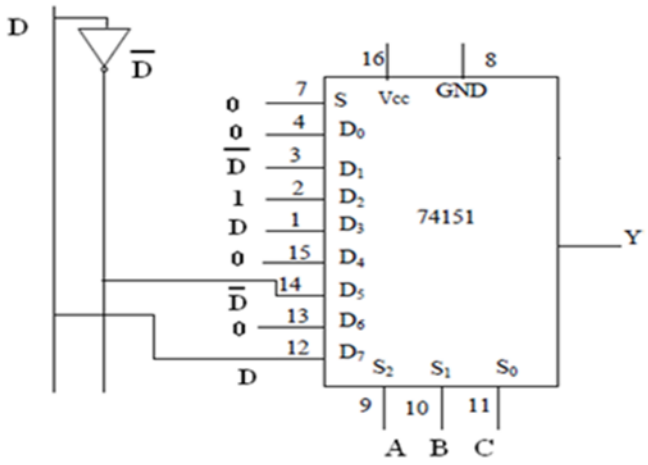


Enable	Select Inputs			Output
E	S2	S1	S0	Y
0	×	×	×	0
1	0	0	0	D0
1	0	0	1	D1
1	0	1	0	D2
1	0	1	1	D3
1	0	0	0	D4
1	0	0	1	D5
1	0	1	0	D6
1	0	1	1	D7

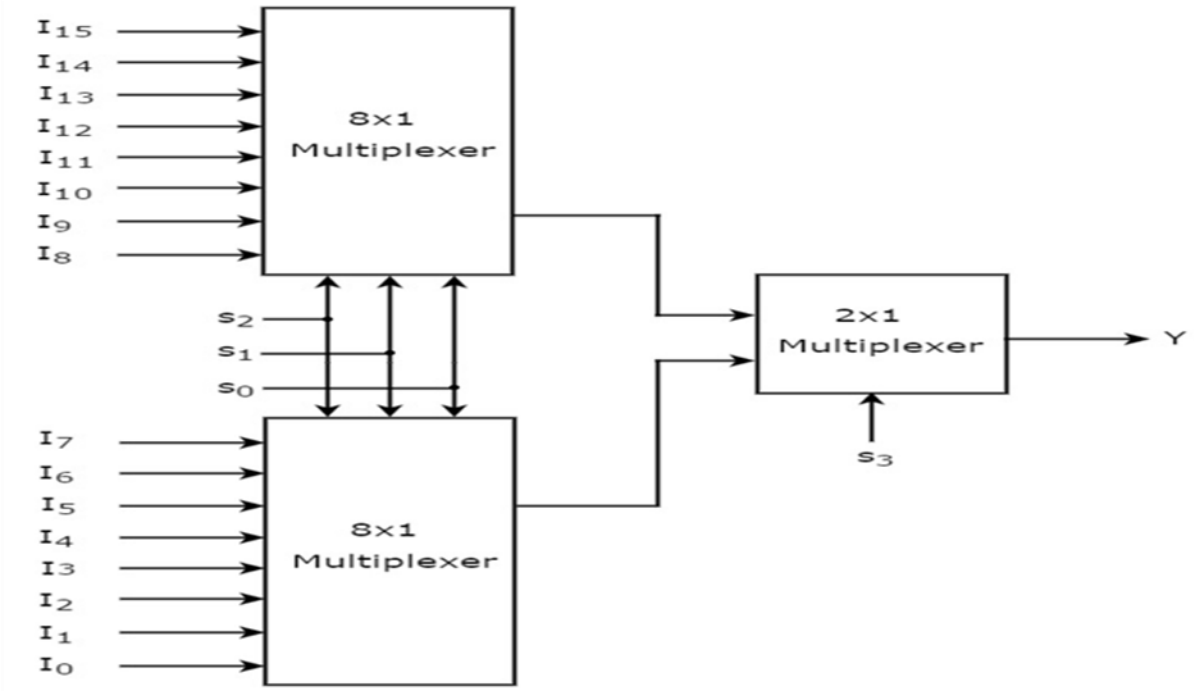
Implementation Table

F=Σm(2,4,5,7,10,14)

	$\overline{D}$	D	
D0	0	1	0
D1	(2)	3	$\overline{D}$
D2	(4)	(5)	1
D3	6	(7)	D
D4	8	9	0
D5	(10)	11	$\overline{D}$
D6	12	13	0
D7	(14)	15	$\overline{D}$

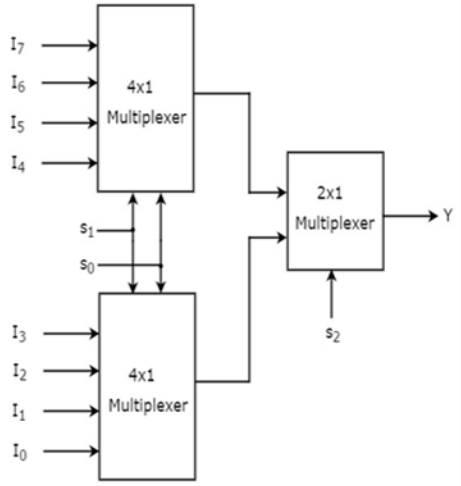


16x1Mux using two 8x1Mux



Cascading of Multiplexers

8x1 Mux using two 4x1Mux



32x1Mux using two 16x1Mux

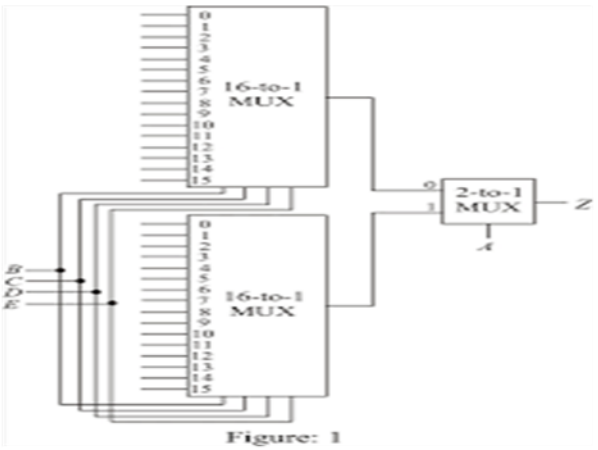
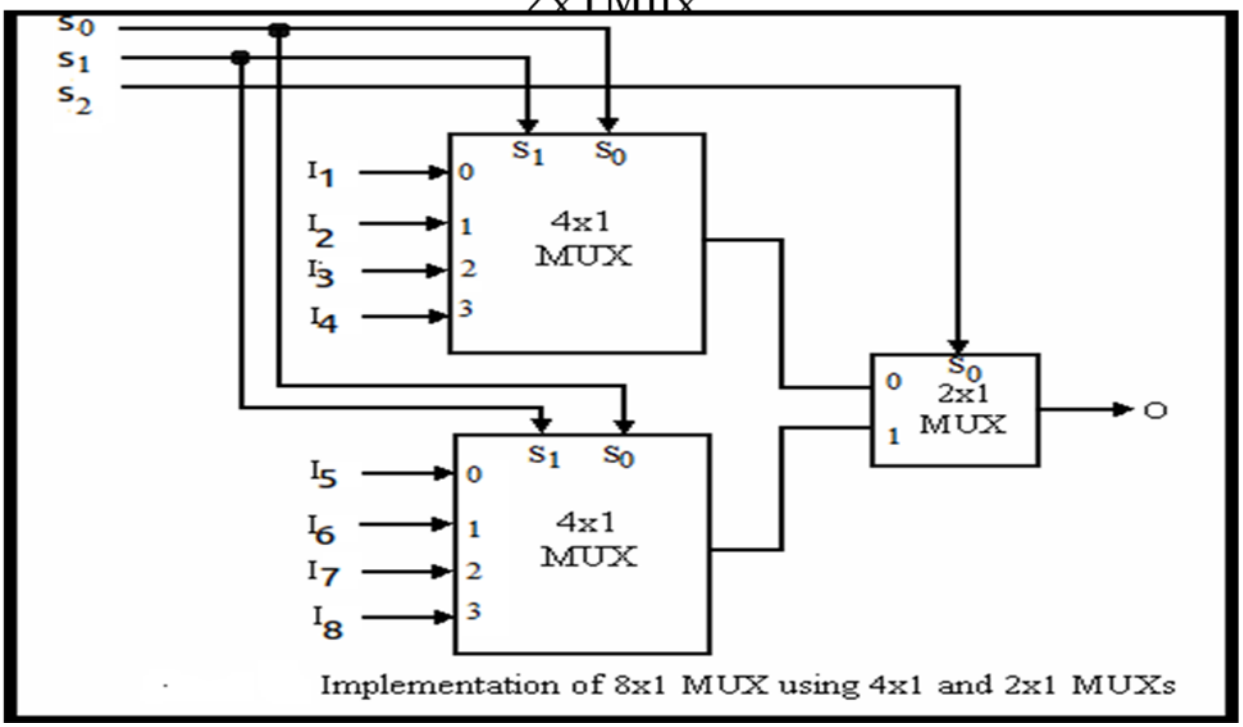


Figure: 1

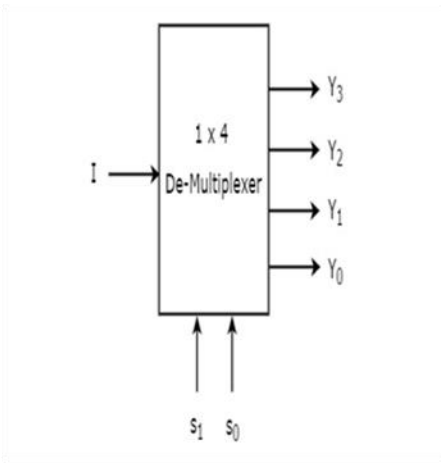
Implementation of 8x1 Mux using 4x1Mux and 2x1Mux



Implementation of 8x1 MUX using 4x1 and 2x1 MUXs

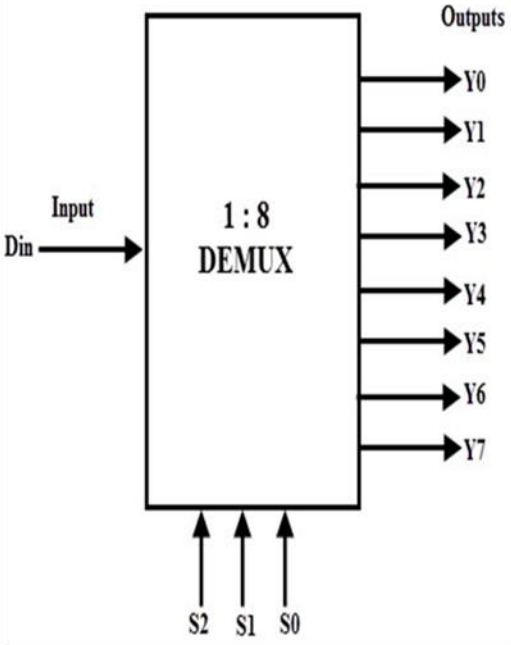
1x4 Demux with Truth Table

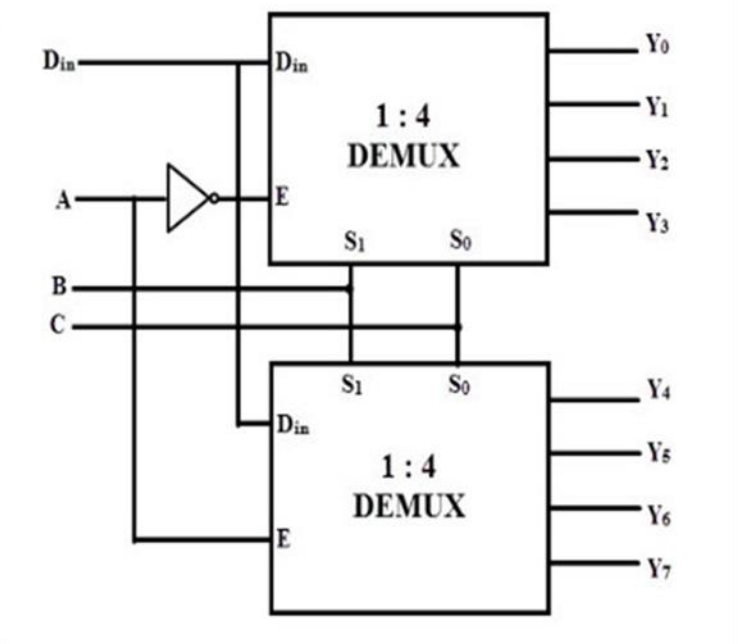
Logic Diagram



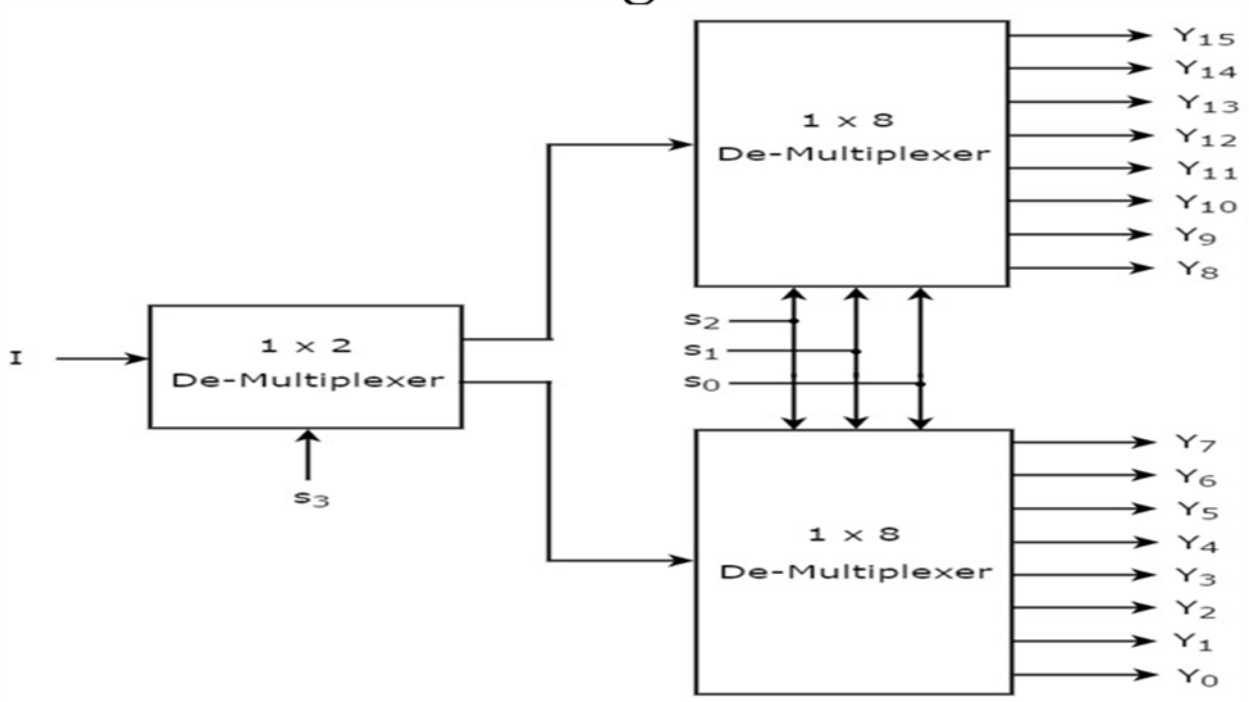
INPUT				OUTPUT			
En	D	S_1	S_0	Y_0	Y_1	Y_2	Y_3
0	X	X	X	0	0	0	0
1	X	0	0	D	0	0	0
1	X	0	1	0	D	0	0
1	X	1	0	0	0	D	0
1	X	1	1	0	0	0	D

1x8 Demux using two 1x4 Demux





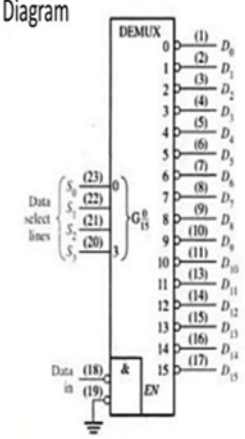
1x16 Demux using two 1x8 Demux



Logic Diagram & Truth Table

1 to 16 line demultiplexer-74154

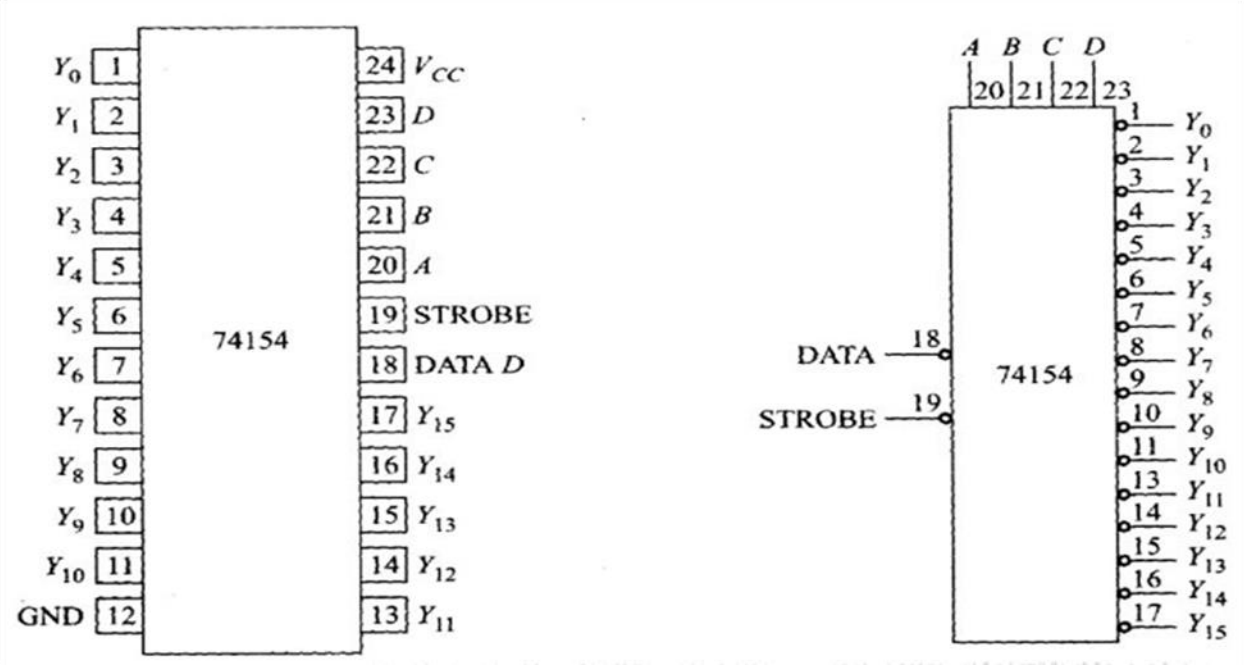
Logic Diagram



INPUTS						OUTPUTS															
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

Pin Diagram & Logic Diagram



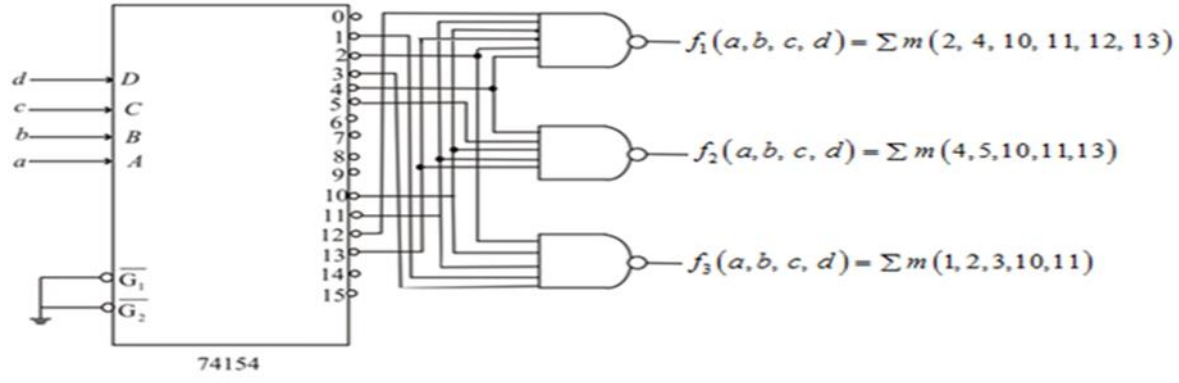
Implementation of multiple functions

$f_1(a,b,c,d) = \sum m(2, 4, 10, 11, 12, 13)$

$f_2(a,b,c,d) = \sum m(4,5,10,11,13)$

$f_3(a,b,c,d) = \sum m(1,2,3,10,11)$

The realization of set of functions with a 74154 decoder module is shown in Figure 1.

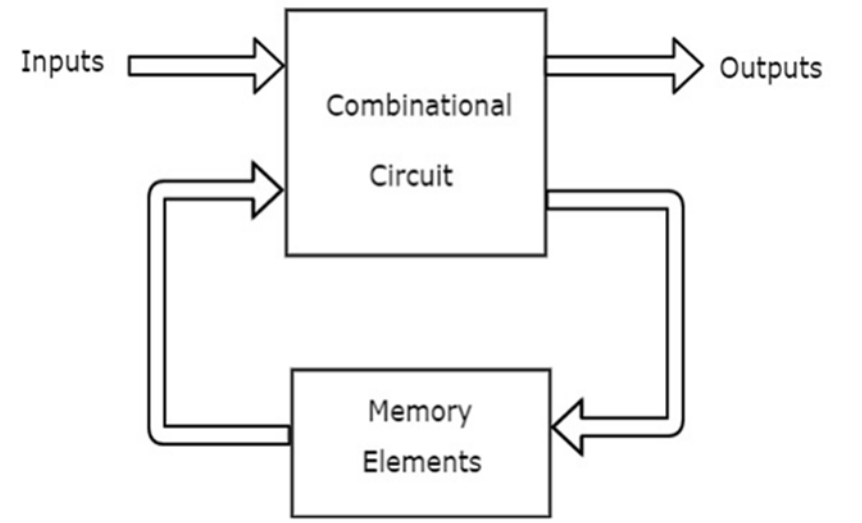


SEQUENTIAL CIRCUITS USING TTL *74XX* ICS

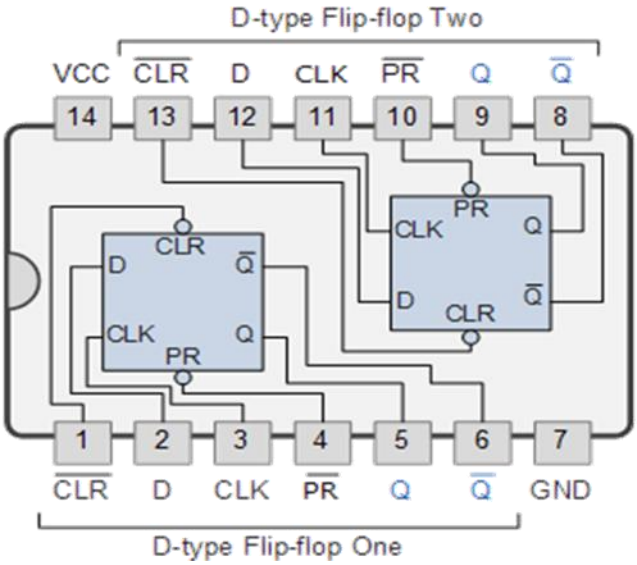
- Flip Flops (IC 7474, IC 7473),
- Shift Registers
- Universal Shift Register(IC 74194)
- 4- bit asynchronous binary counter(IC 7493).

Sequential Circuit

Block Diagram



D Flip Flop (IC7474)



CLR – Clears the output to zero

PR – Sets the output to one

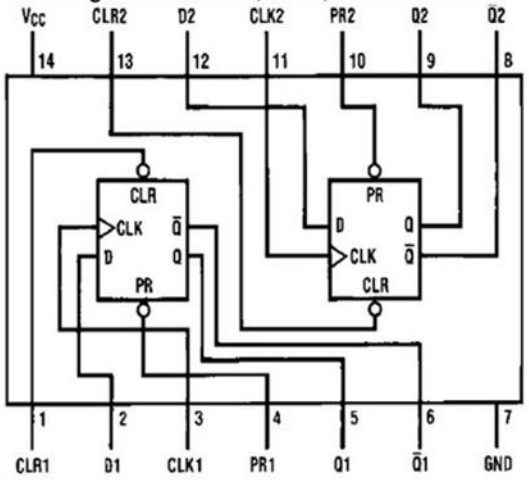
Dual Functionality

Q & Q⁻ are the Complimentary outputs.

Truth Table of D Flip Flop

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



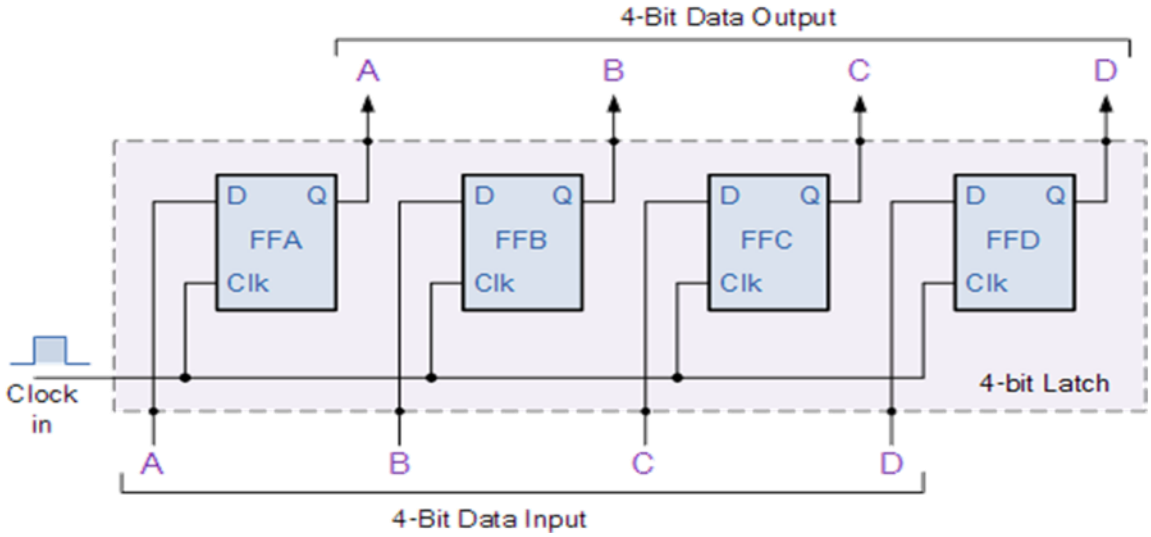
Truth Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}$ 0

Note: Q0 = the level of Q before the indicated input conditions were established.

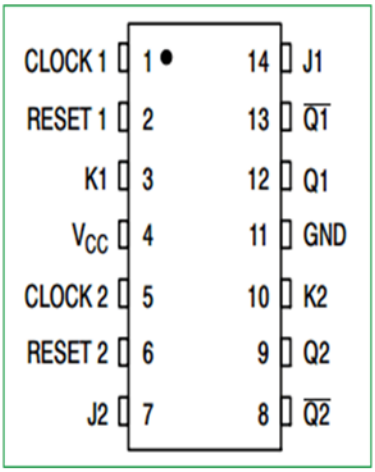
Note 1: This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (HIGH) level.

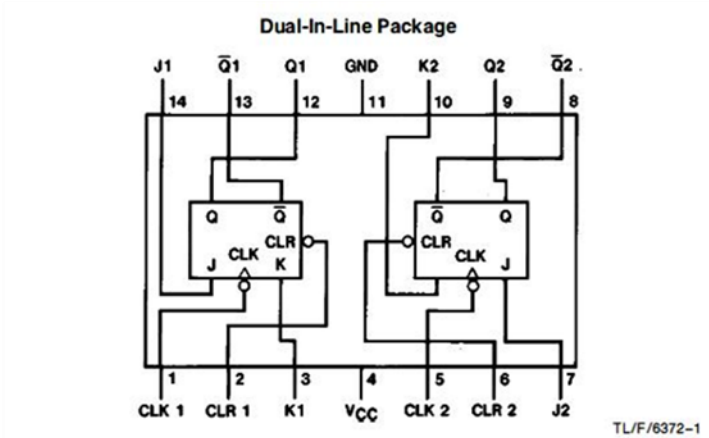
Delay Flip Flop (4-Bit Data Input)



IC7473 (JK Master Slave Flip Flop)

Pin Diagram

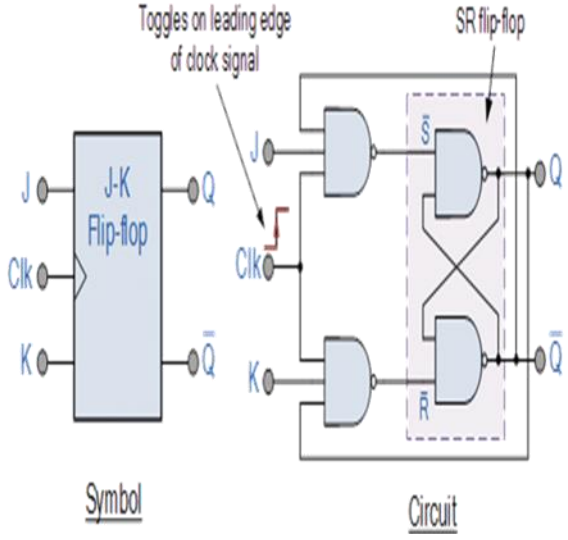




Order Number DM54LS73AJ, DM54LS73AW, DM74LS73AM or DM74LS73AN
See NS Package Number J14A, M14A, N14A or W14B

J-K Master Slave Flip-Flop(IC7473)

J-k Flip Flop

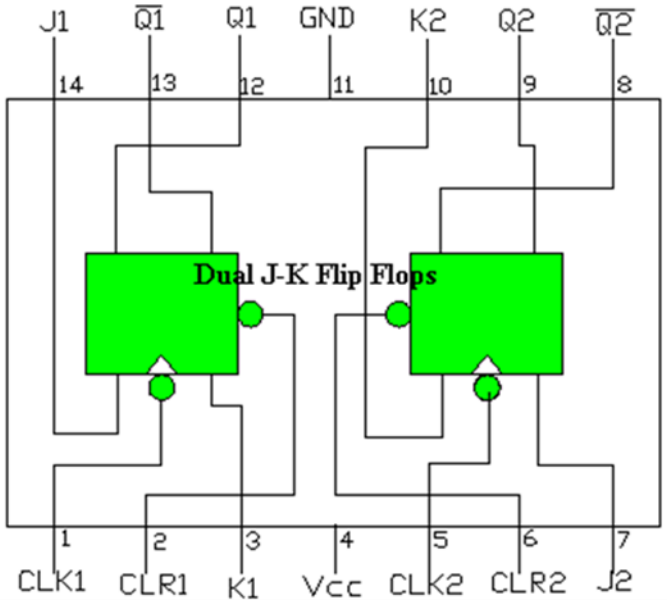


Truth table

CLR	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	H	L	H
H	↓	H	L	H	L
H	↓	L	L	Retains previous state	
H	↓	H	H	Toggle	

Pin Diagram & Truth table

Connection Diagram



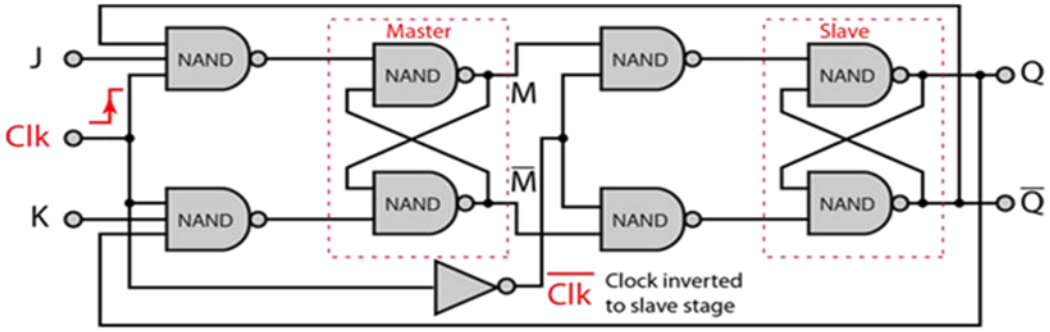
Function Table

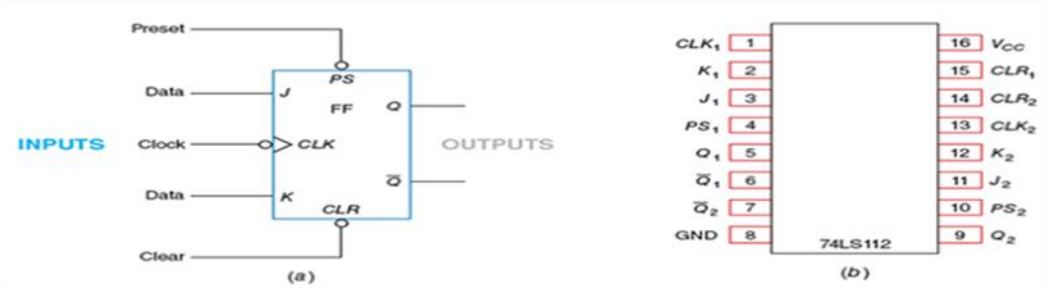
Inputs				Outputs	
CLR	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\bar{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	

H = HIGH Logic Level
L = LOW Logic Level
X = Either LOW or HIGH Logic Level
↓ = Positive pulse data, the J and K inputs must be held constant while the clock is HIGH. Data is transferred to the outputs on the falling edge of the clock pulse.
Q_0 = The output logic level before the indicated input conditions were established.
Toggle = Each output changes to the complement of its previous level on each HIGH level clock pulse.

Connection Diagram

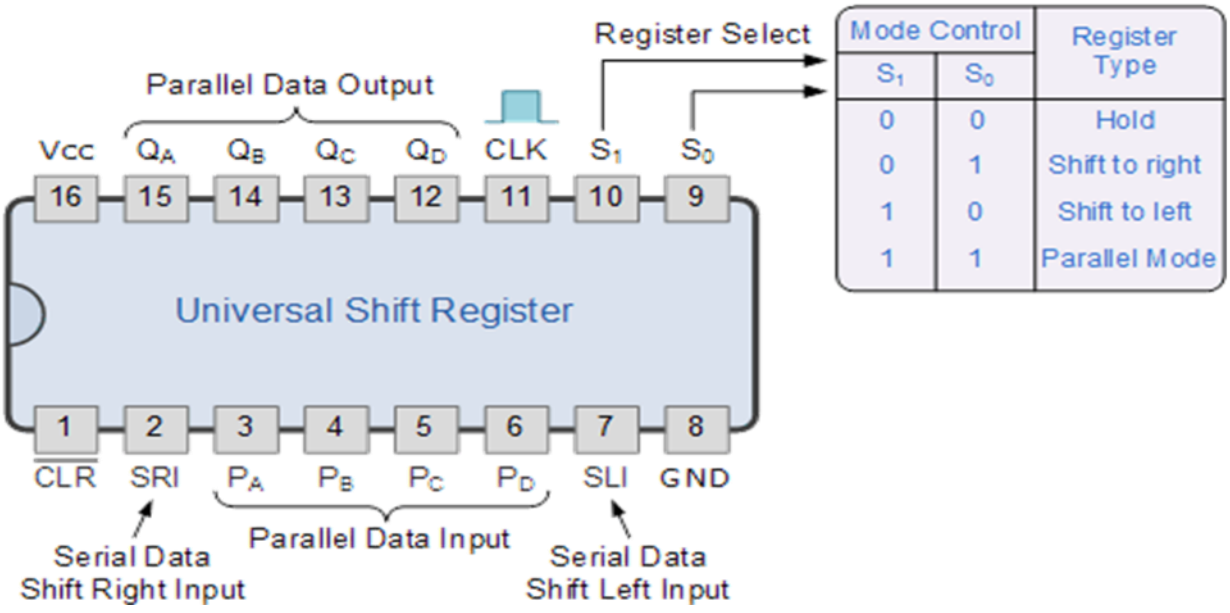
J-K Master Slave Flip-Flop





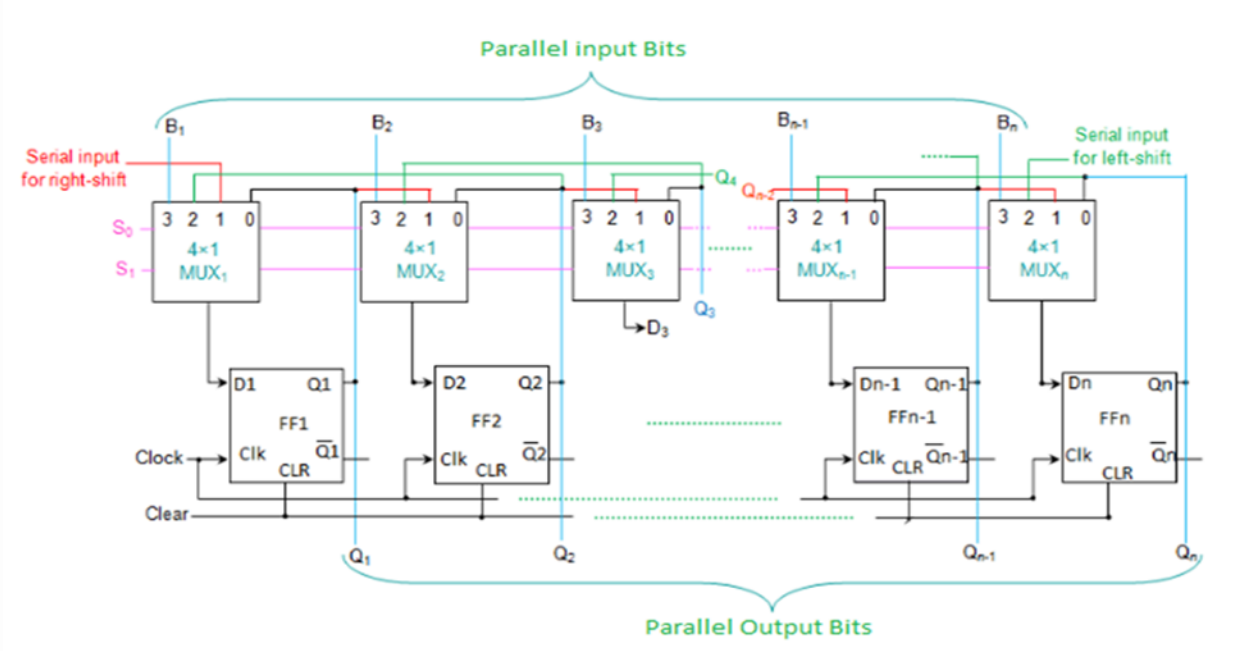
Universal Shift Register (IC74194)

Pin Diagram

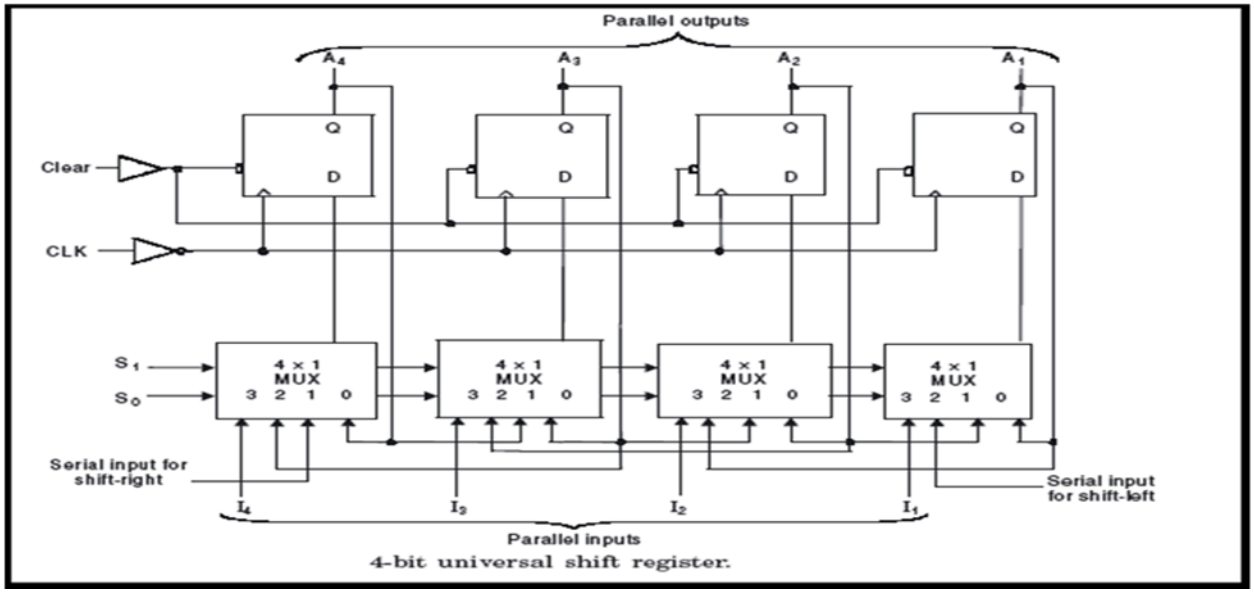


Mode Control		Register Type
S_1	S_0	
0	0	Hold
0	1	Shift to right
1	0	Shift to left
1	1	Parallel Mode

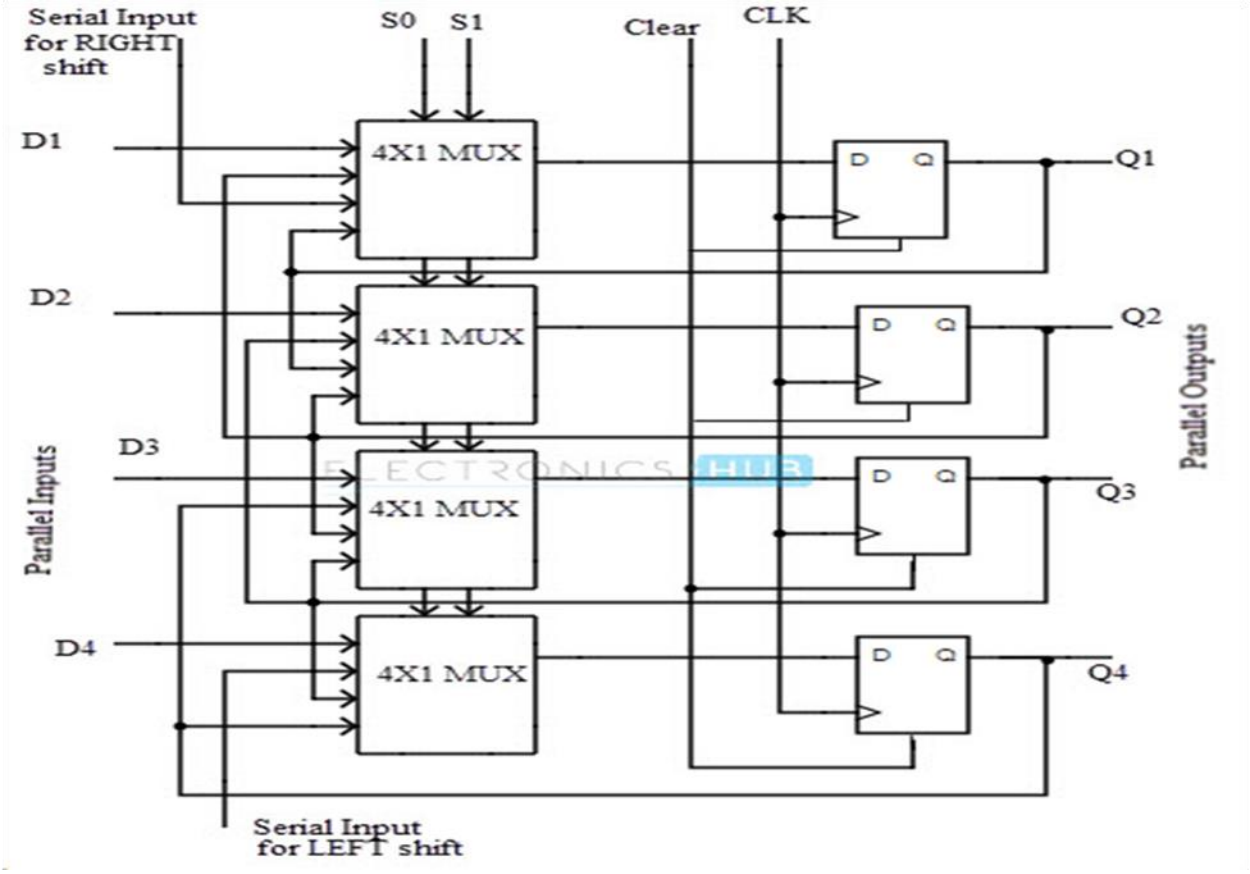
Universal Shift Register



Operation of USR

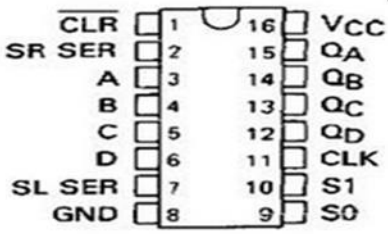


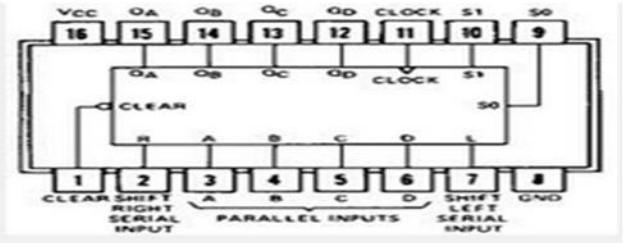
4-bit universal shift register.



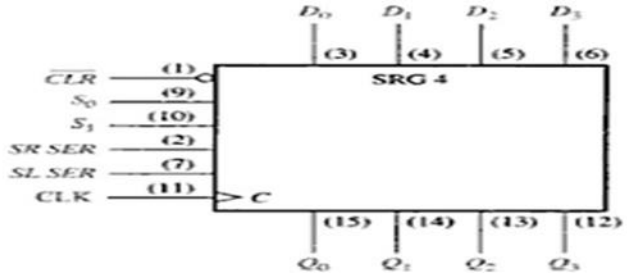
Universal Shift Register(IC 74HC194)

Pin Diagram

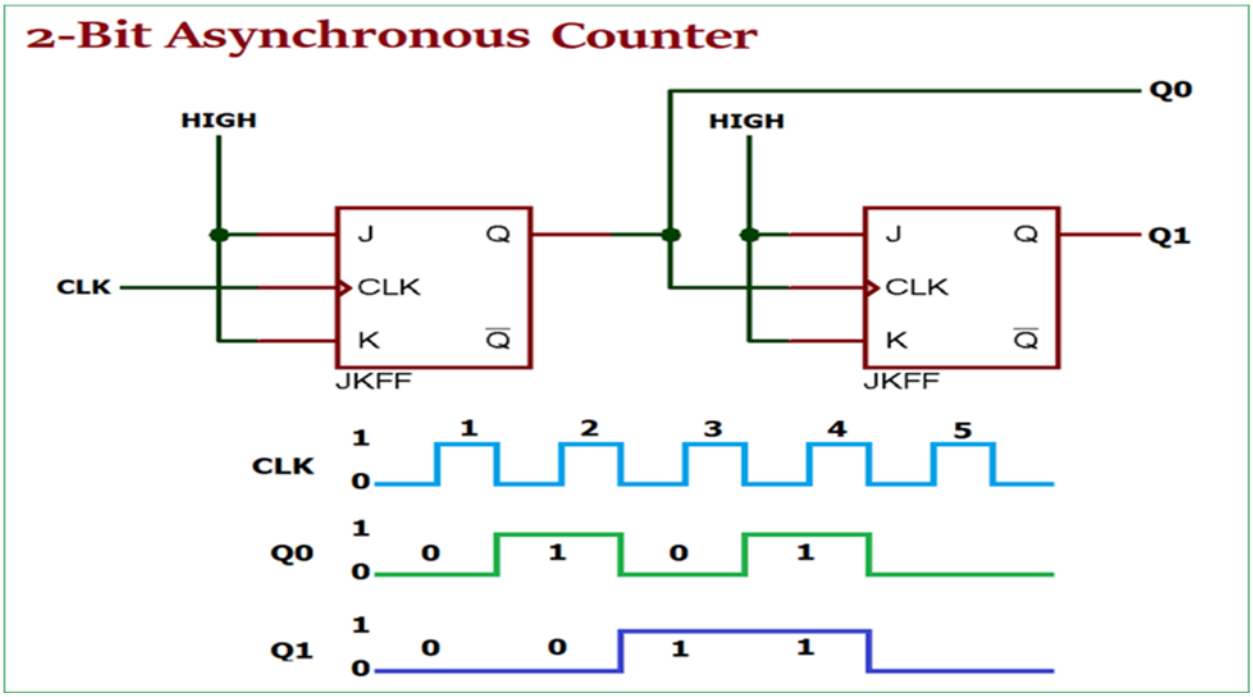




Logic Diagram

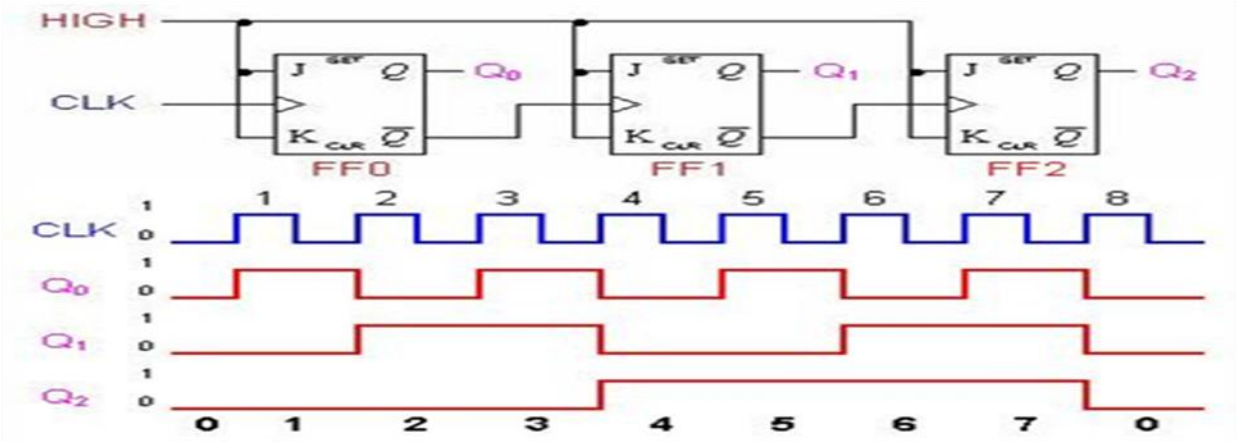


Asynchronous Counter



Asynchronous Counter

3-Bit Asynchronous Binary Counter

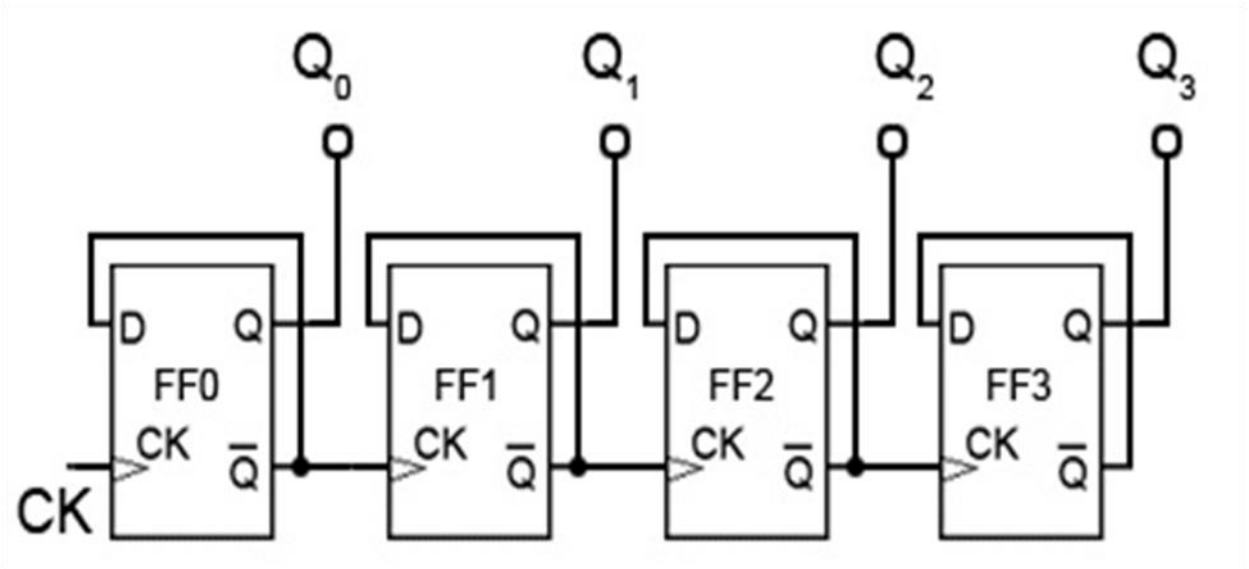


3-Bit Asynchronous Binary Counter

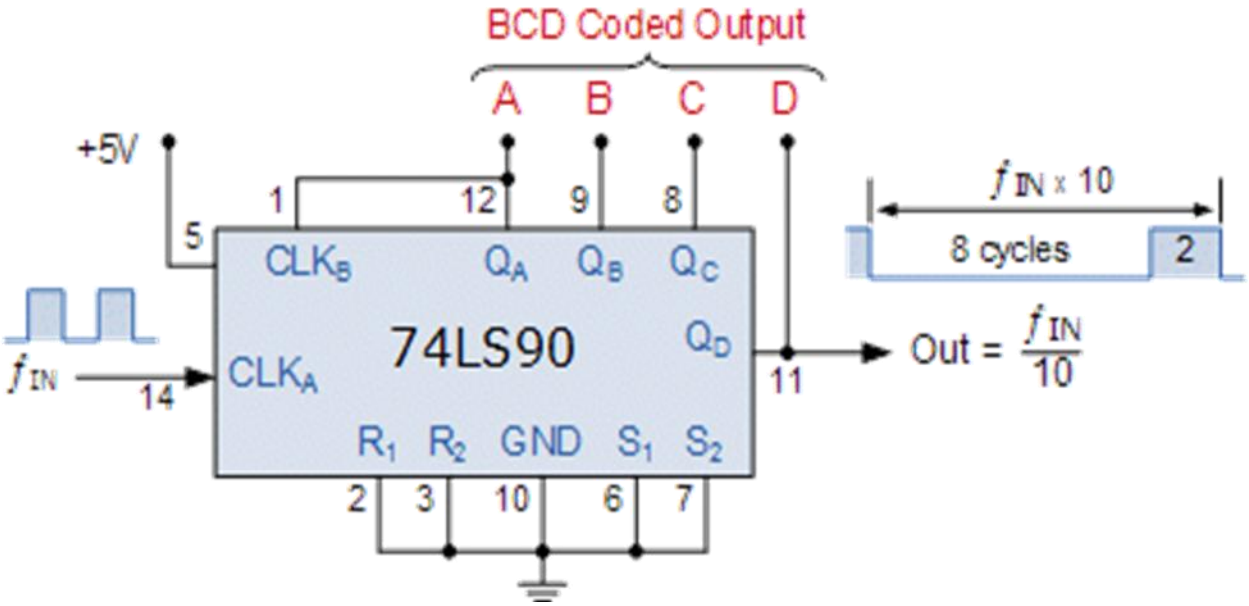
Truth Table

Counter State	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

Block Diagram



4-Bit Decade Counter



4-Bit Decade Counter

Block Diagram